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YX70 M/B Schematics Document

AMD-Rembrandt-FP7r2_BGA1140 with DDR5 + NV N20 E3/E5 GPU

2021-05-22

REV: 1.0

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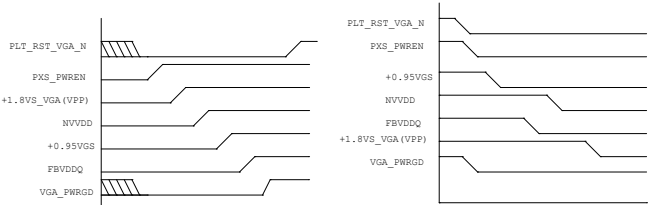
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GN20x-E GPIO

GPIO	I/O	GPIO Name	Function Description	Net name	I/O Termination
GPIO0	OUT	NVVDD_PWM_VID	PWM Output to control NVVDD	NVVDD_PWM_VID	
GPIO1	OUT	GC6:GC6_FB_EN	FB Enable for GC6	FB_GC6_EN (10K PD)	
GPIO2	IN	GC6:GPU_EVENT*	Wake the GPU from GC6 state	GPU_EVENT#_R (10K PU)	
GPIO3	OUT	DISP_MUX_CNTL	Display MUX control signal	GPU_MUX_CNTL (10K PD)	
GPIO4	OUT	MSVDD_EN	GPU power sequencing for GC6 ---MSVDD_EN	GPIO4_GC6_MSVDD_EN (10K PU)	
GPIO5	OUT	FRAME_LOCK*	Active low Frame Lock for NVSR panel	UNUSED	
GPIO6	OUT	NVVDD_PSI*	Phase Shedding, NVVDD_PSI	NVVDD_PSI (10K PU) RSVD	
GPIO7	OUT	LCD_BL_PWM	LCD Panel Backlight PWM	GPU_EDP_PWM (100K PD)	
GPIO8	OUT	MEM_VDD_CTL	Memory voltage Control	FBVDDQ_SEL (10K PD)	
GPIO9	I/O	THERM_ALERT*	Active Low Thermal Alert	VGA_ALERT# (10K PU)	
GPIO10	OUT	MEM_VREF_CTL	Memory VREF Control	MEM_VREF_CTL (100K PD)	
GPIO11	OUT	LCD_VDD	LED Panel power enable	GPU_EDP_ENVDD (10K PD)	
GPIO12	IN	PWR_LEVEL	AC power detect or power supply overdraw input	VGA_AC_DET_R (10K PU)	
GPIO13	IN	IGPU_BL_EN	Signal indicating when the IGPU has EN the BL	IGPU_EDP_ENBKLL (100K PU)	
GPIO14	IN	HPD_IFPA*	Hot Plug Detect for IFPA	IFPA_HPD (10K PU)	
GPIO15	IN	HPD_IFPB*	Hot Plug Detect for IFPB	IFPB_HPD (10K PU)	
GPIO16	OUT	DISP_MUX_PWM_CNTL	Allows switching the PWM between IGPU & DGPU	PWM_SW_SELECT (10K PD)	
GPIO17	IN	HPD_IFPD*	Hot Plug Detect for IFPD	GPU_EDP_HPD (10K PU)	
GPIO18	IN	HPD_IFPE*	Hot Plug Detect for IFPE	UNUSED	
GPIO19	OUT	UNUSED			
GPIO20	OUT	UNUSED			
GPIO21	OUT	LCD_BLEN	LCD Panel Backlight Enable	GPU_EDP_ENBKLL (100K PD)	
GPIO22	OUT	ADC_MUX_SEL	OVRM MUX Input SEL	ADC_MUX_SEL (2.2K PU)	
GPIO23	OUT	UNUSED	UNUSED		
GPIO24	IN	HPD_IFPF*/USBC_HPD* or DONGLE_DET*	Hot Plug Detect for IFPF or USBC	UNUSED	
GPIO25	OUT	FBVDD_PSI	Turns off phases of the Frame buffer power supply	FBVDDQ_PSI (5.1K PU)	
GPIO26	OUT	ROM_WP* FP_FUSE	Connect to WP pin of the GPU EEPROM N18P-G61-A Control FP_FUSE	GPIO26_ROM_WP (10K PD) GPIO26_FP_FUSE (10K PD) RSVD	
GPIO27	IN	HPD_IFPC*	Hot Plug Detect for IFPC	IFPC_HPD (10K PU)	
GPIO28	OUT	MSVDD_PWM_VID	PWM Output to CNTL MSVDD	UNUSED	
GPIO29	OUT	NVVDD_EN	NVVDD Enable RSVD	GPIO29_NVVDD_EN (100K PU) RSVD	
GPIO30	OUT	MSVDD_PSI*	Phase Shedding	UNUSED	

GN20x-E Power Sequence



1. The ramp time for any rail must be more than 40us and is recommended to be less than 2ms.
2. It is recommended that the delay from IVS on to PEXVDDQ/PGVDD assertion not exceed 20ms.
3. The ramp-up overshoot should not exceed the silicon reliability limit voltage.
4. Power up NVVDD must be 90% before PEXVDD can sleep-up.
5. Refer to the JEDEC Memory SPBC for memory-related power sequencing.
7. FBVDDQ, USB_VDDP and IVS_AOM don't need power cycle for GC6

1. For GDDR6, VPP must be equal to or higher than FBVDDQ at all times; use gate logic and discharge circuit as needed.
2. All 3.3V devices that connect to the GPU must be ramp down before IVS; GPU can NOT have any 3.3V leakage path after IVS power down.
3. Power down of PEXVDD must be less than 10% before NVVDD can start ramp-down.

H=High: Tied to 1.8V

M=Middle: Tied to 0.9V

L=Low: Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG4-0J	GN20x-E VRAM
L	L	L	0 (0x0000)	Samsung K4Z803258C-HC14
L	L	H	1 (0x0001)	Micron MT61K256M32JE-14-A
L	H	L	2 (0x0002)	Hynix H56C8H24AIR-S2C
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	M	8 (0x0008)	
L	M	L	9 (0x0009)	Samsung (or E7) K4ZAF3258M-HC 14
L	M	H	10 (0x000A)	
L	H	M	11 (0x000B)	
M	L	L	12 (0x000C)	
M	L	H	13 (0x000D)	

FS_OVERT# FUNCTION

ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT# FUNCTION
L	L	H	FS_OVERT# function ENABLE
L	L	L	FS_OVERT# function DISABLED Reserved, do not configure

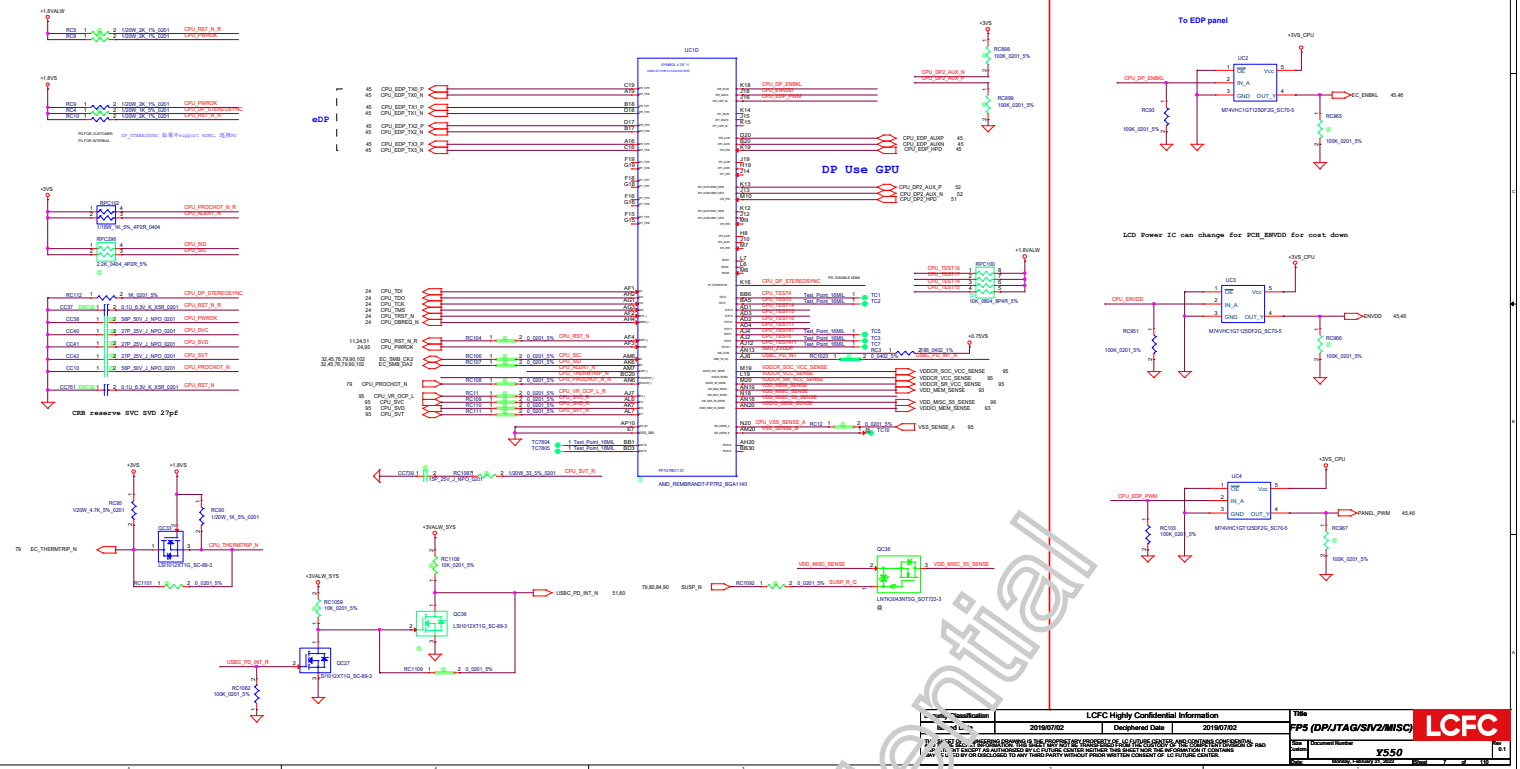
BOM Structure Control Table

BOM Structure	BTO Item
8	Not stuff
OPT#	GN20-E7/E5/E3 Stuff
NON E3#	GN20-E3 No Stuff

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	1	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

- 1:SMB_ALT_ADDR ENABLE
- 0:SMB_ALT_ADDR DISABLE
- 1:DEVID_SEL REBRAND
- 0:DEVID_SEL ORIGINAL
- 1:PCIE_CFG LOW POWER
- 0:PCIE_CFG HIGH POWER
- 1:VGA_DEVICE ENABLE
- 0:VGA_DEVICE DISABLE

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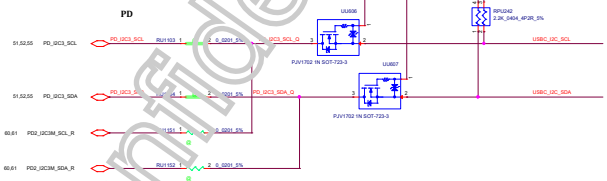
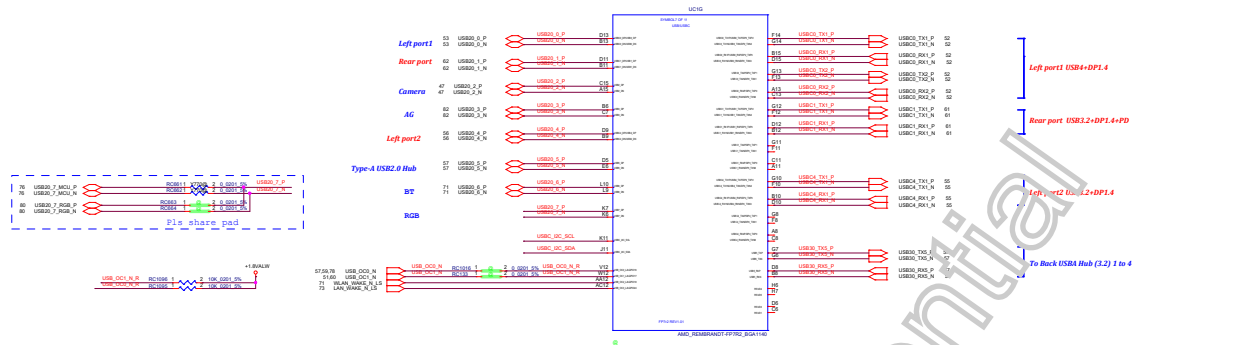
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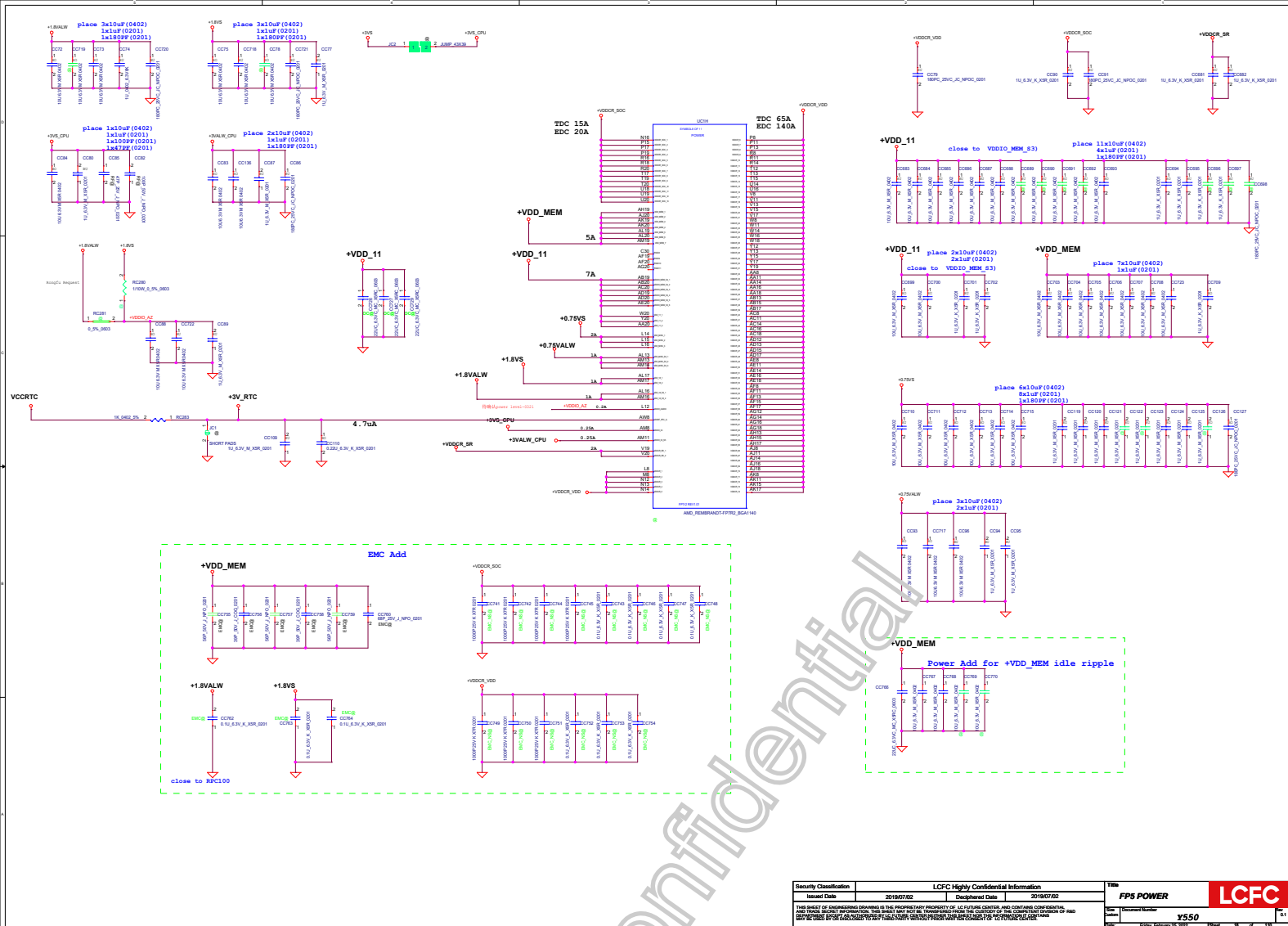
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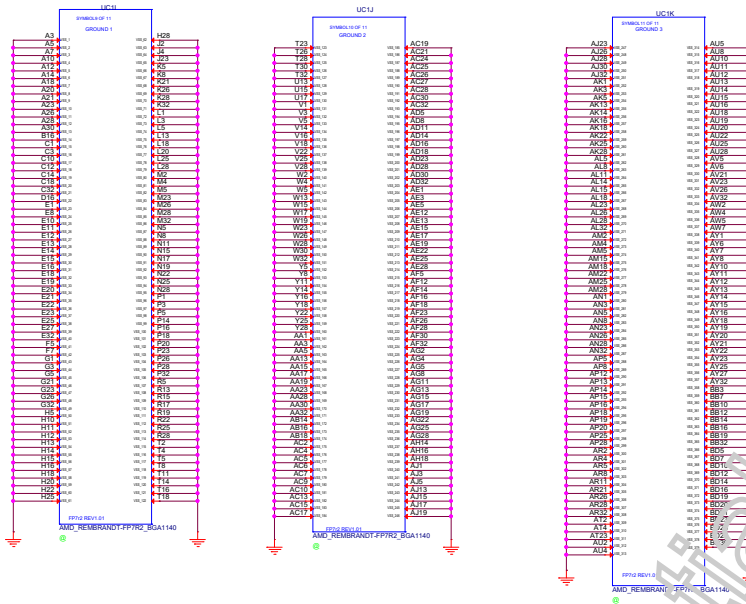
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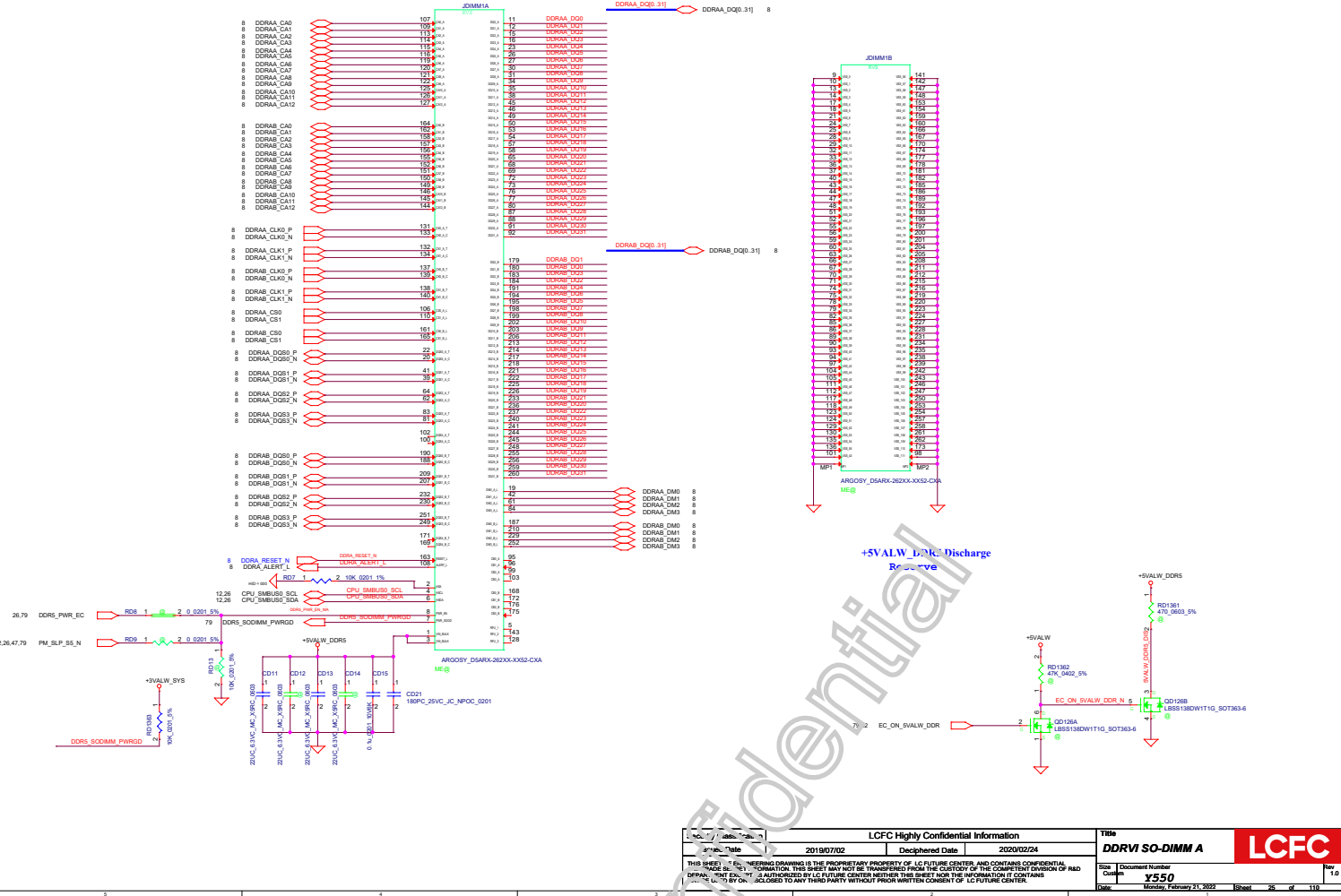


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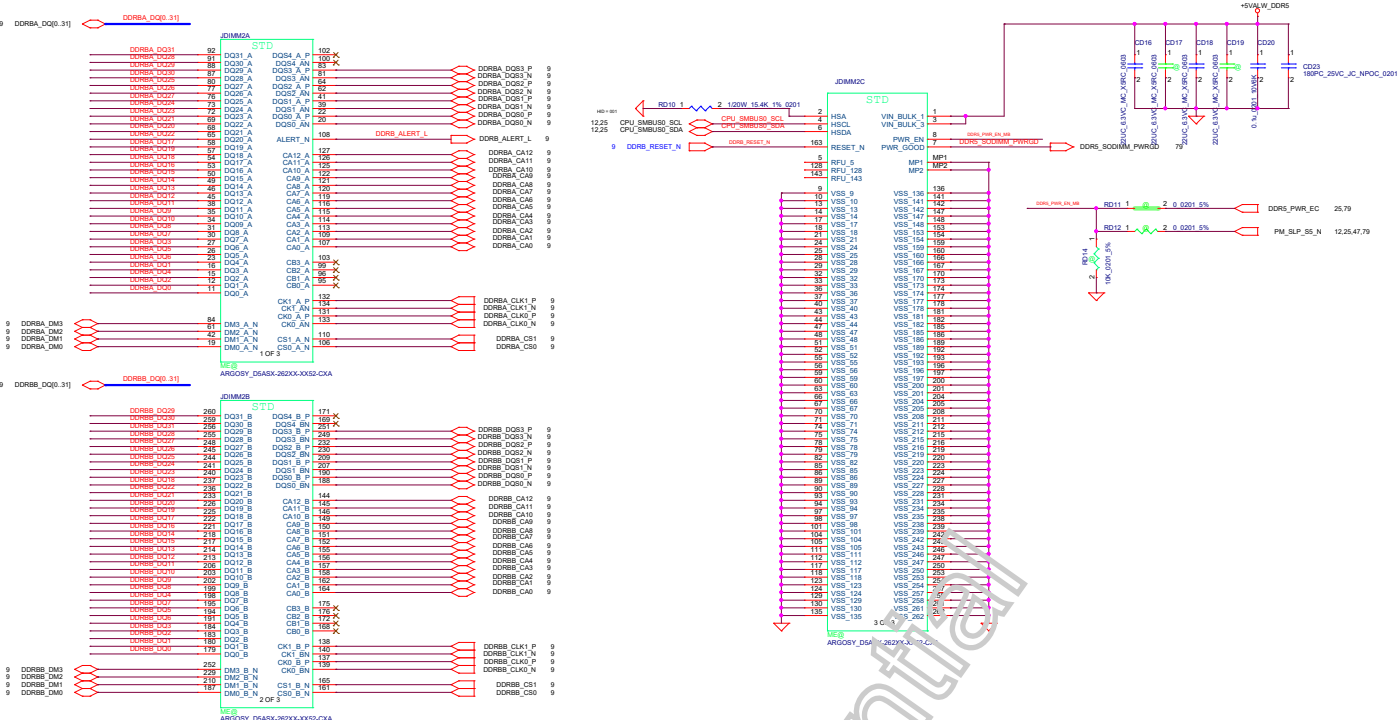
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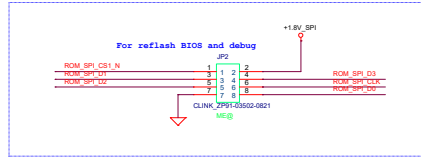
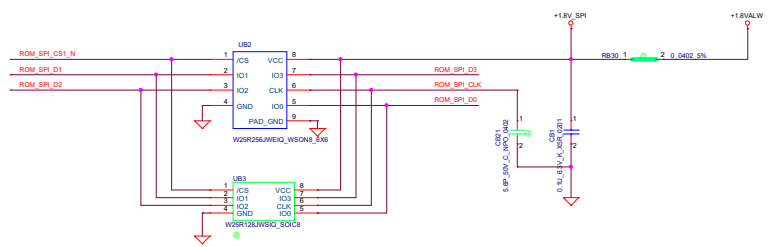
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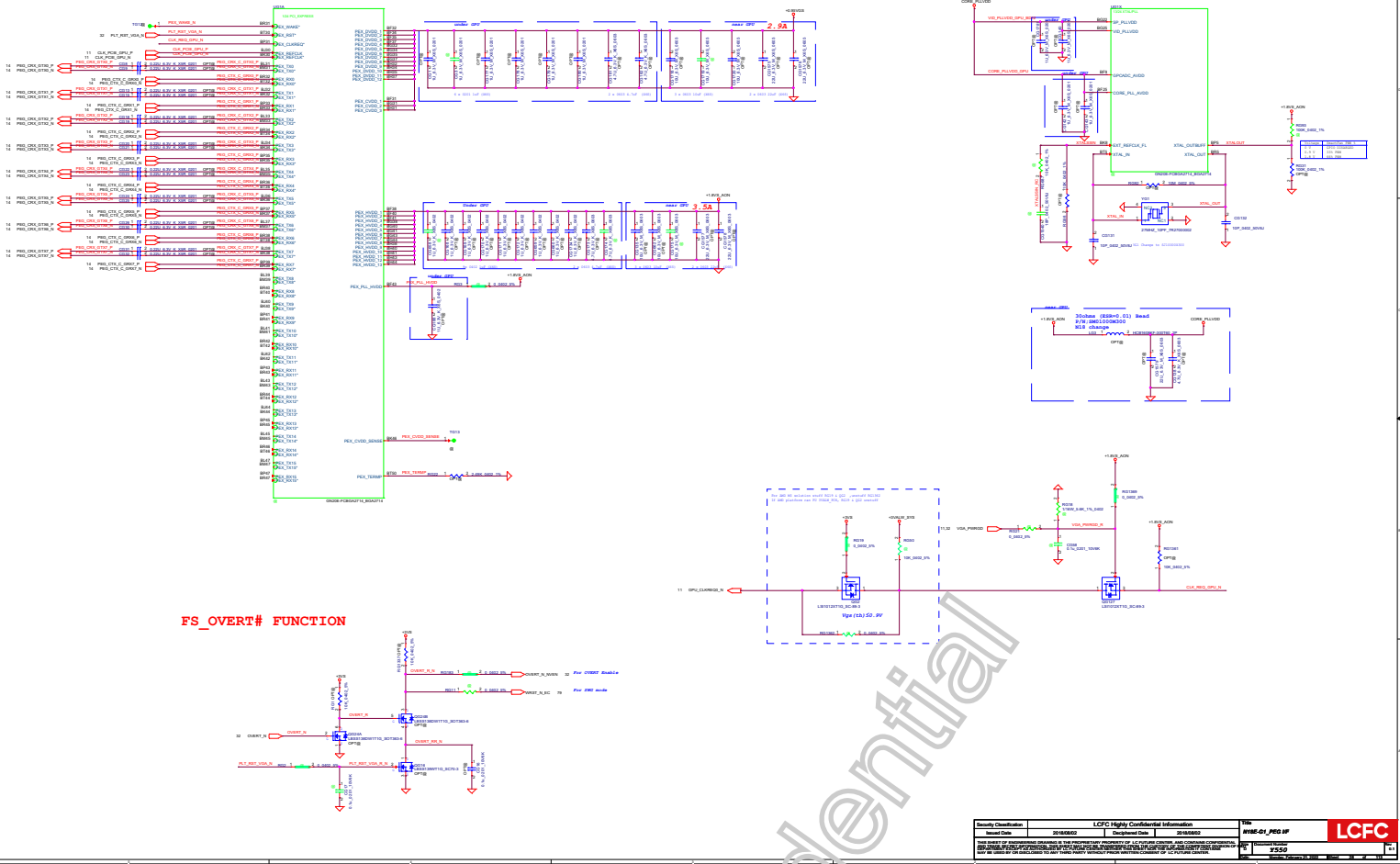


11	CPU_SPL_CS1_N	RB20	2	1	0.0402 5%	ROM_SPL_CS1_N
11	CPU_SPL_D0	RB21	2	1	0.0402 5%	ROM_SPL_D0
11	CPU_SPL_D1	RB22	2	1	0.0402 5%	ROM_SPL_D1
11	SPL_CLK	RB23	2	1	0.0402 5%	ROM_SPL_CLK
11	CPU_SPL_D2	RB24	2	1	0.0402 5%	ROM_SPL_D2
11	CPU_SPL_D3	RB25	2	1	0.0402 5%	ROM_SPL_D3
79	EC_SPL_CS1_N	RB13	1	2	0.0201 5%	CPU_SPL_CS1_N
79	EC_SPL_CLK	RB27	1	2	0.0201 5%	SPL_CLK
79	EC_SPL_SI	RB28	1	2	0.0201 5%	CPU_SPL_D0
79	EC_SPL_SO	RB29	1	2	0.0201 5%	CPU_SPL_D1

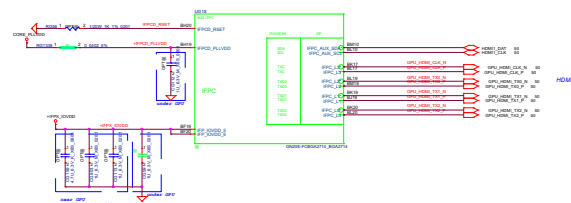


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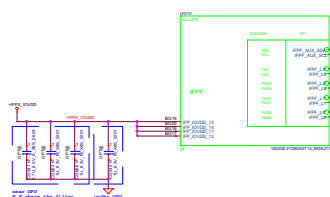
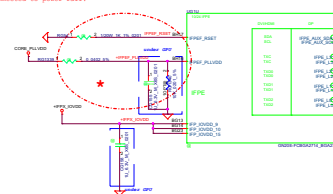
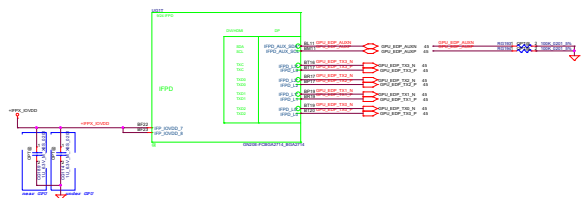


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Part Number			AT86GS-PDS-IP
Part Name			5550
Part Description			5550



1.If an IFP link is unused, The main and AUX links, IFPxy_RSDT can be left unconnected, and IFPxy_PLIVED should be 10K PD to GND.

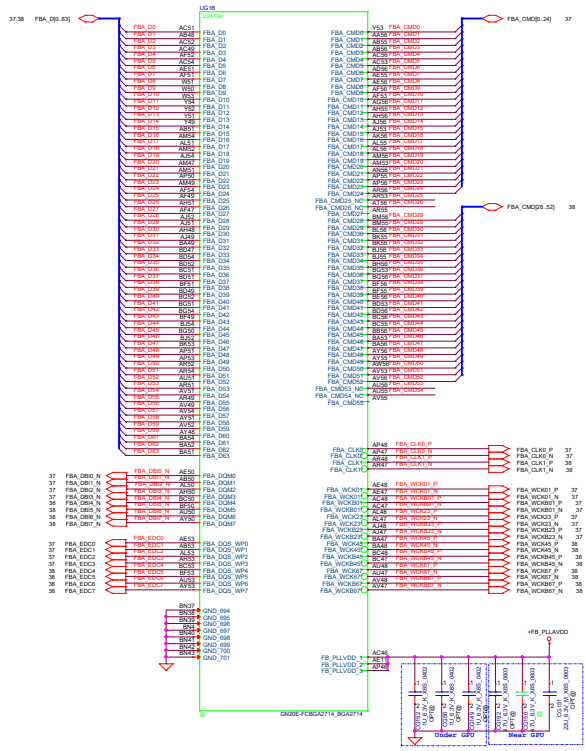
2.IFP_IOWD rail can be left unconnected if no IFP link is used. If any IFP is used, all IFP_IOWD balls must be connected to power rail.



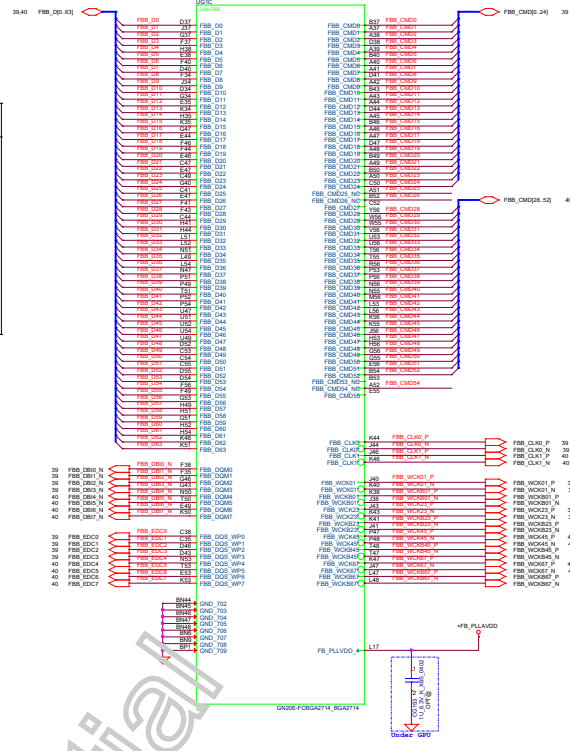
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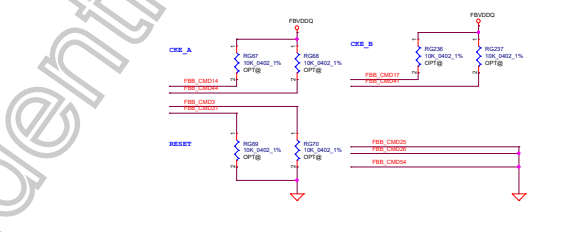
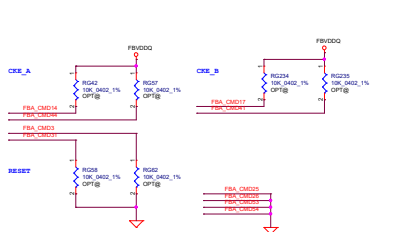
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10	Y550



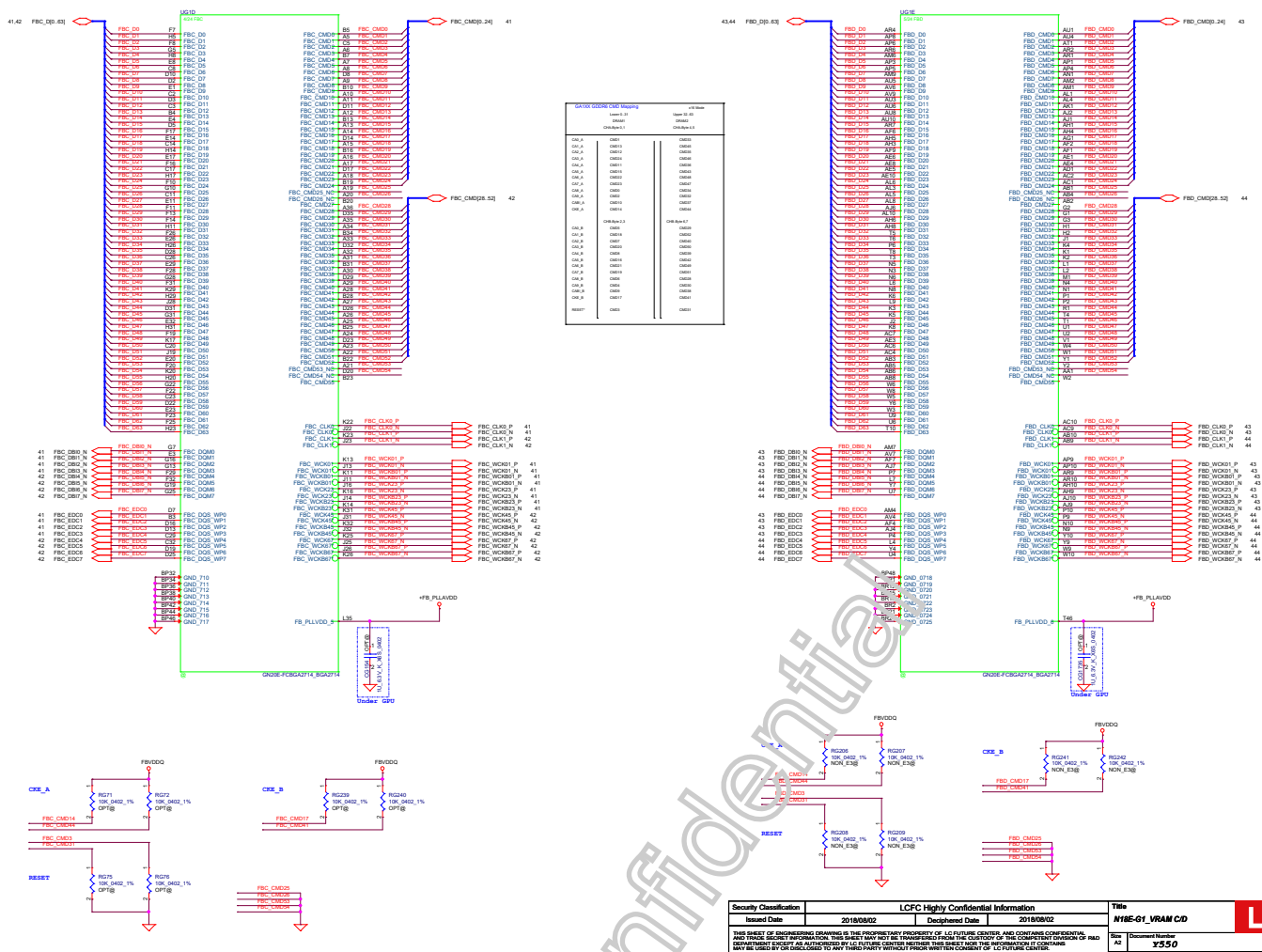
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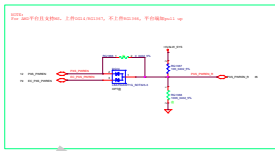
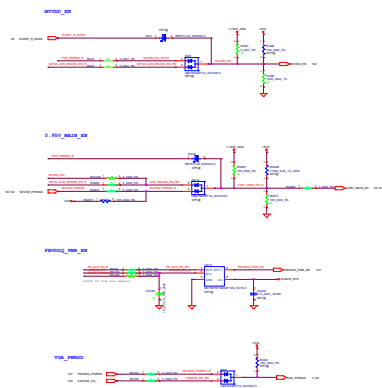
30ohm (ESR=0.01) Bead
P/N: SMC1000M300
WLS: 0.01mm



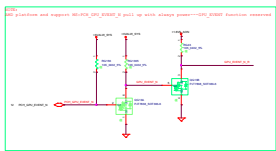
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Rev		Rev		Rev	



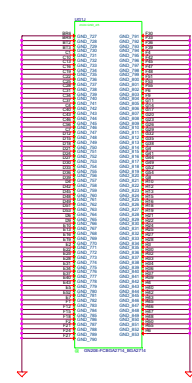
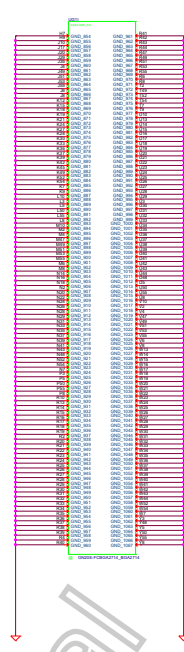
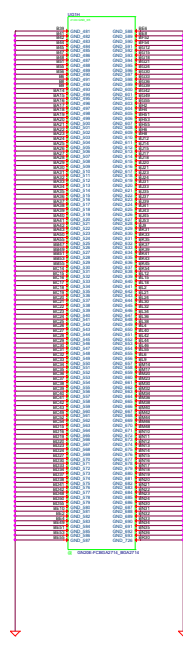
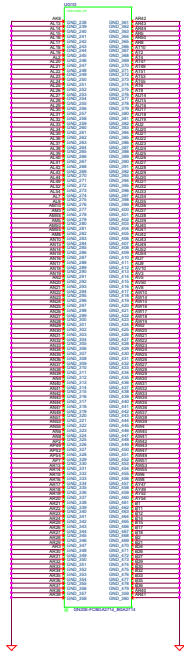
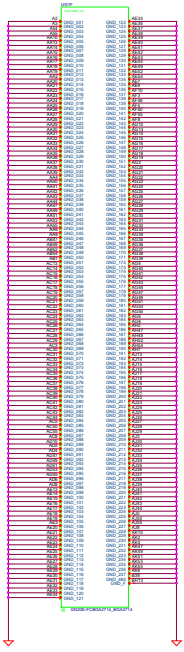
Power on/off sequence



Discharge



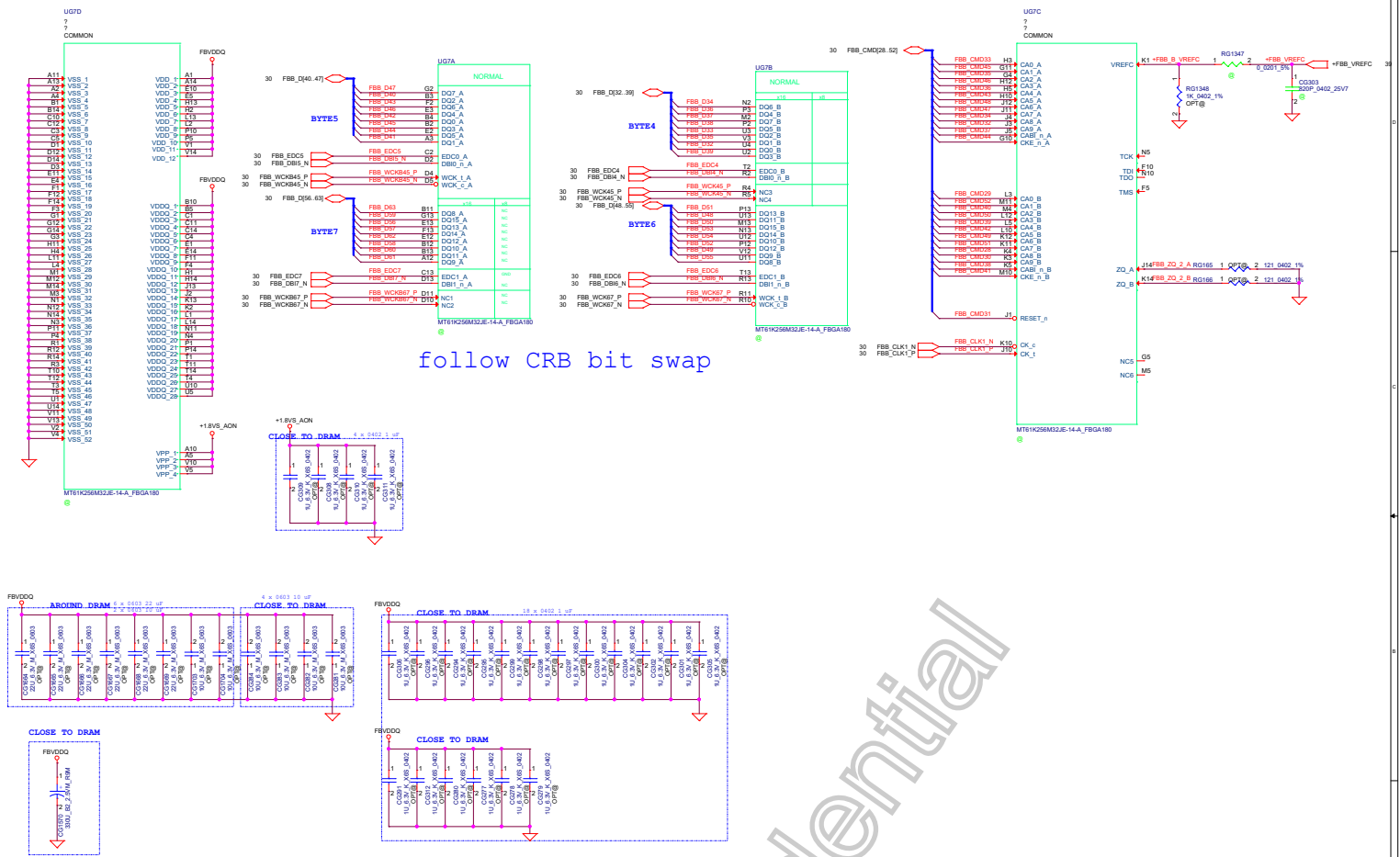
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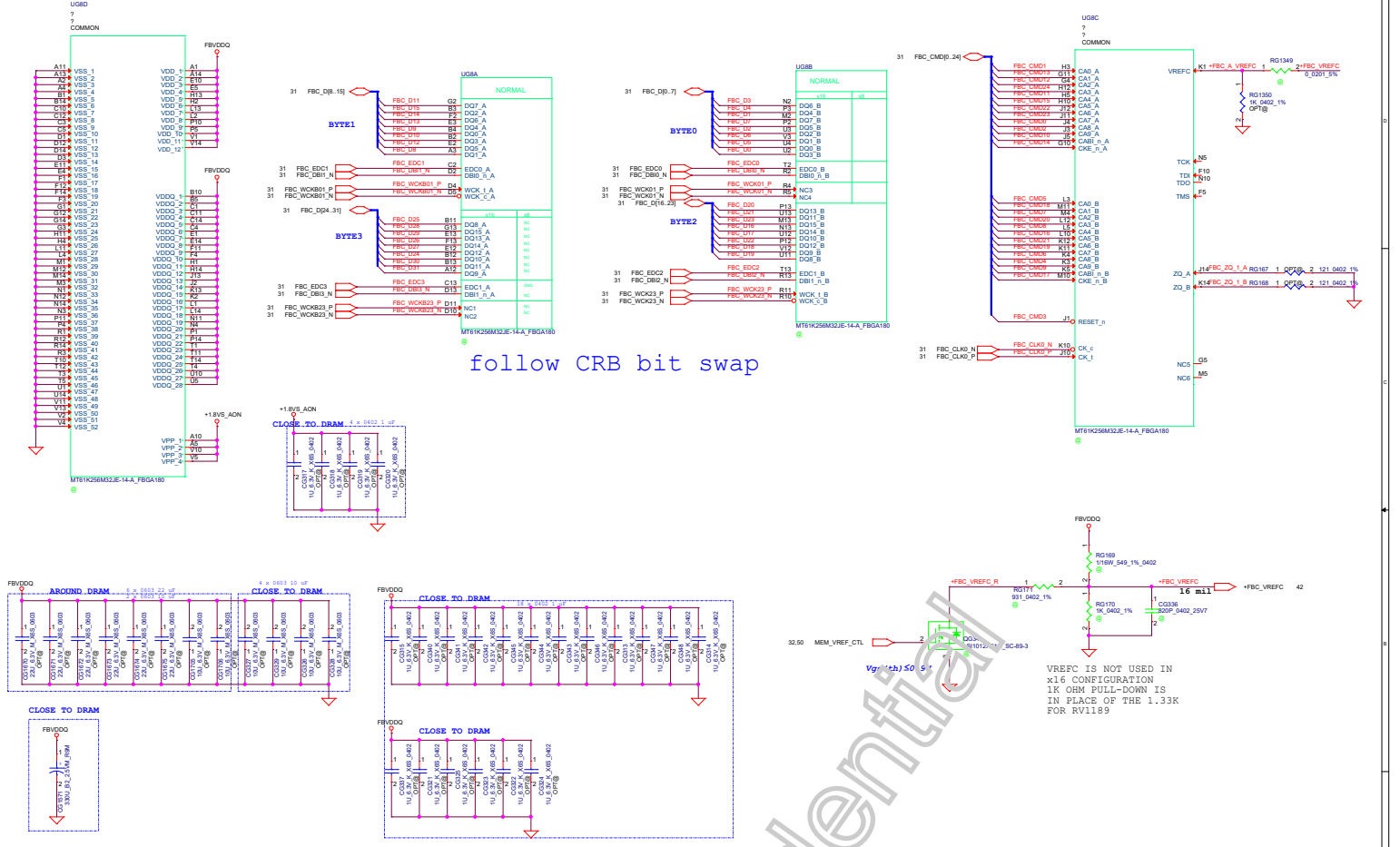
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follow CRB bit swap

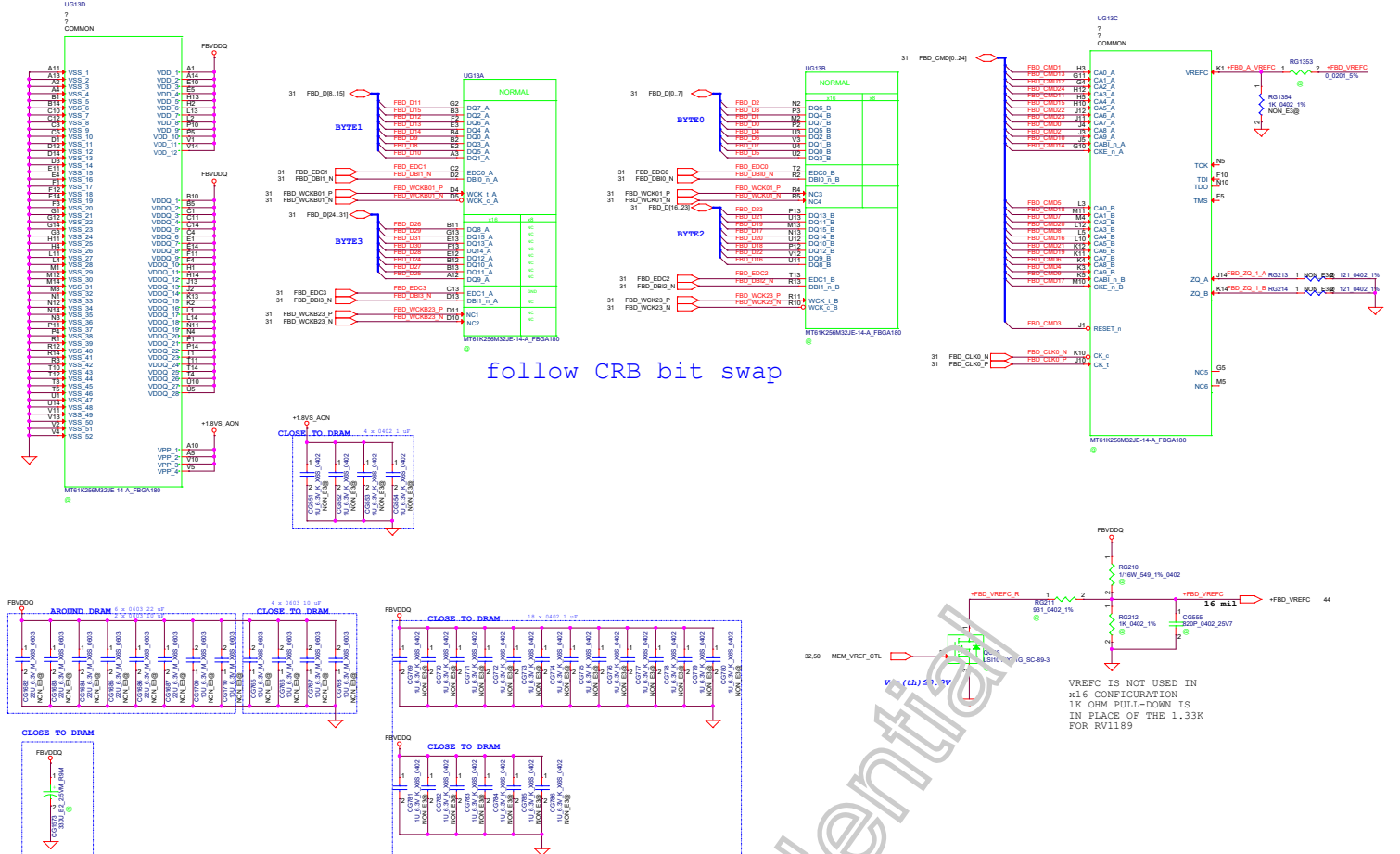
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				Date	Monday, February 21, 2023
				Sheet	35 of 115



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Doc Number	Y550		Rev
Doc	Y550		0.1
Date	Monday, February 21, 2023	Sheet	45 of 115



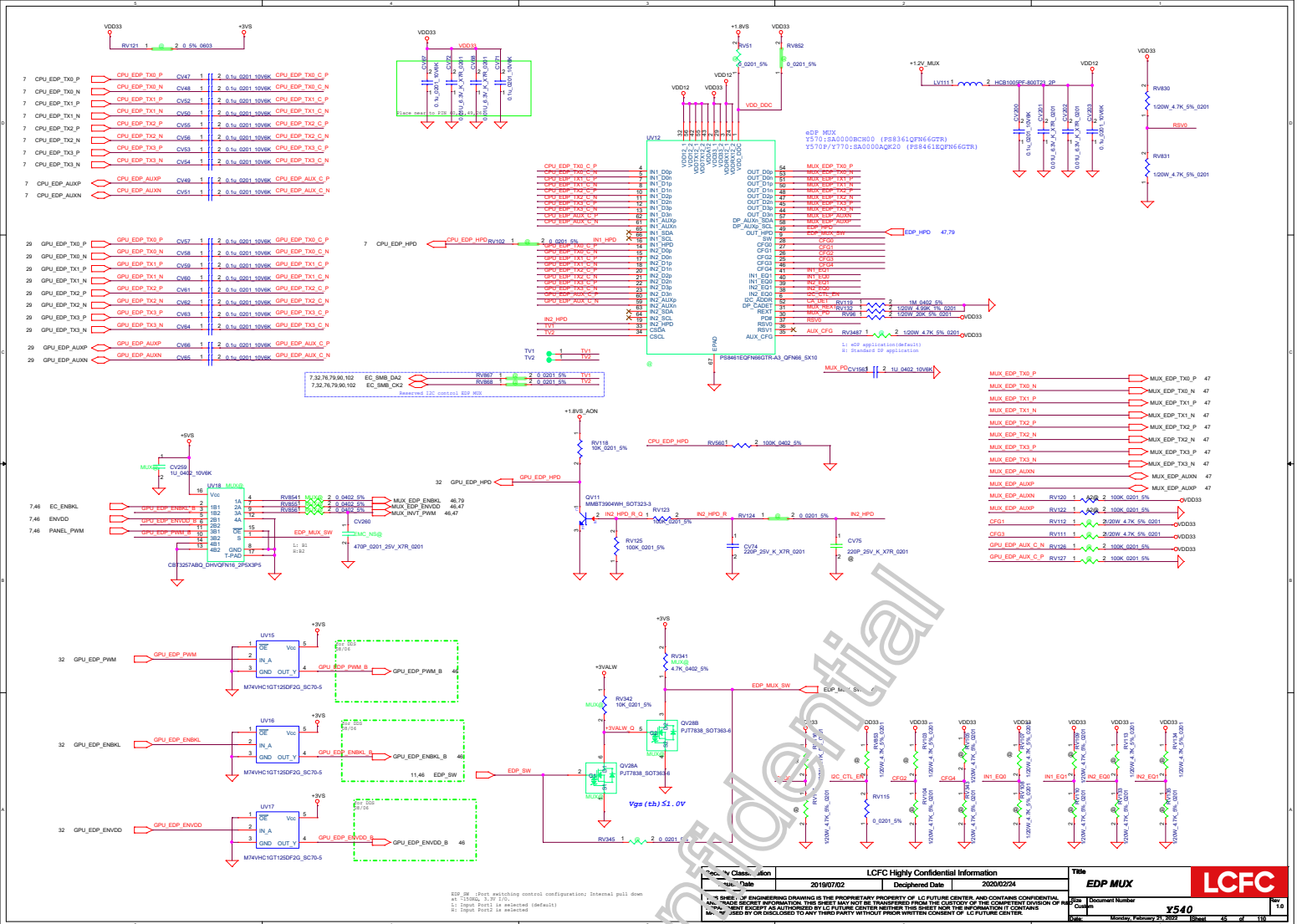
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Doc No	Y550		Rev 0.1
Date	Monday, February 21, 2023	Sheet	41 of 115

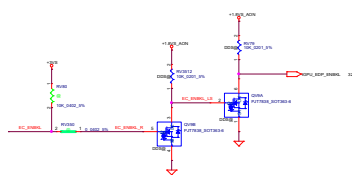
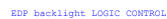
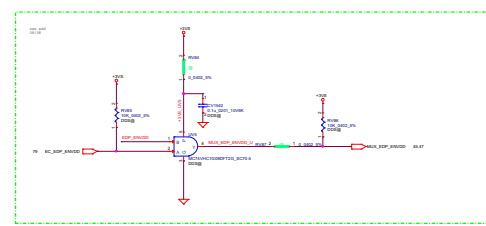
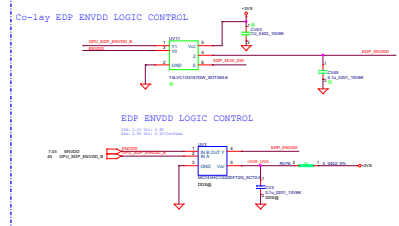
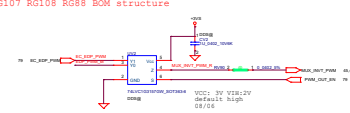
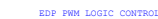
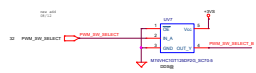


follow CRB bit swap

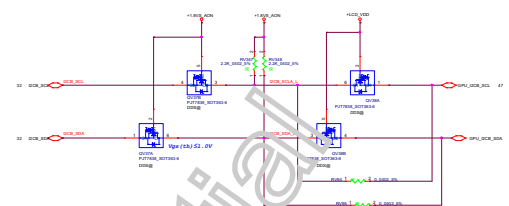
VREFC IS NOT USED IN
X16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR RV1189

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Doc No	Y550	Rev	0.1
Date	Monday, February 21, 2018	Sheet	45 of 115





Del E-sport



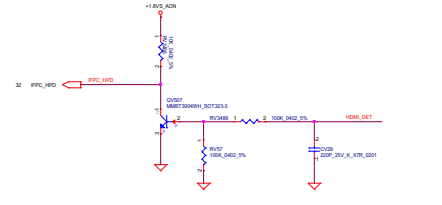
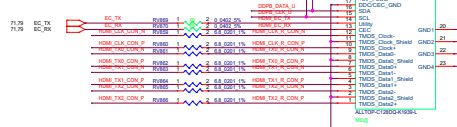
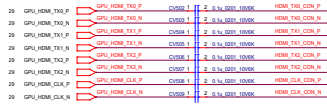
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Page		1		Document Number	
				Y540	

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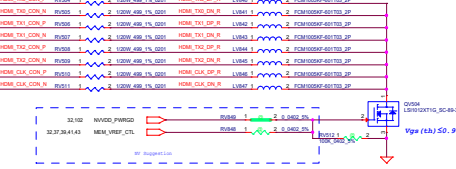
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Revised Date	20080302	Disciplined Date		
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156				156

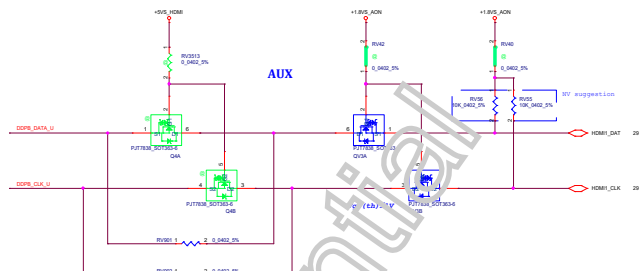
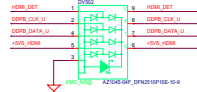
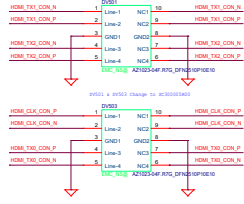
HDMI Power



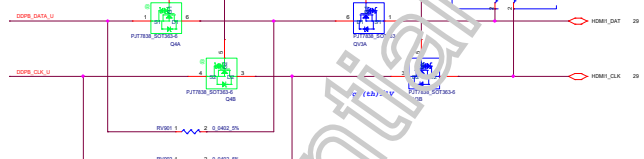
CPU_HDMI_HPD Pull high voltage change to +1.8VALLW from +1.8VS



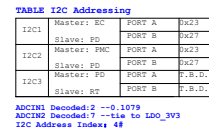
EMC



AUX

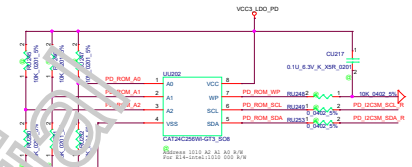
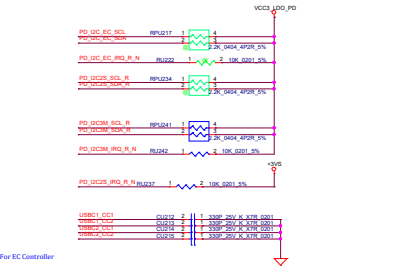


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Revision	20180702	Decompile	20180702	
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File Name	Y560	Page	1	1
Date	Monday, February 27, 2018	Time	10:10	10:10

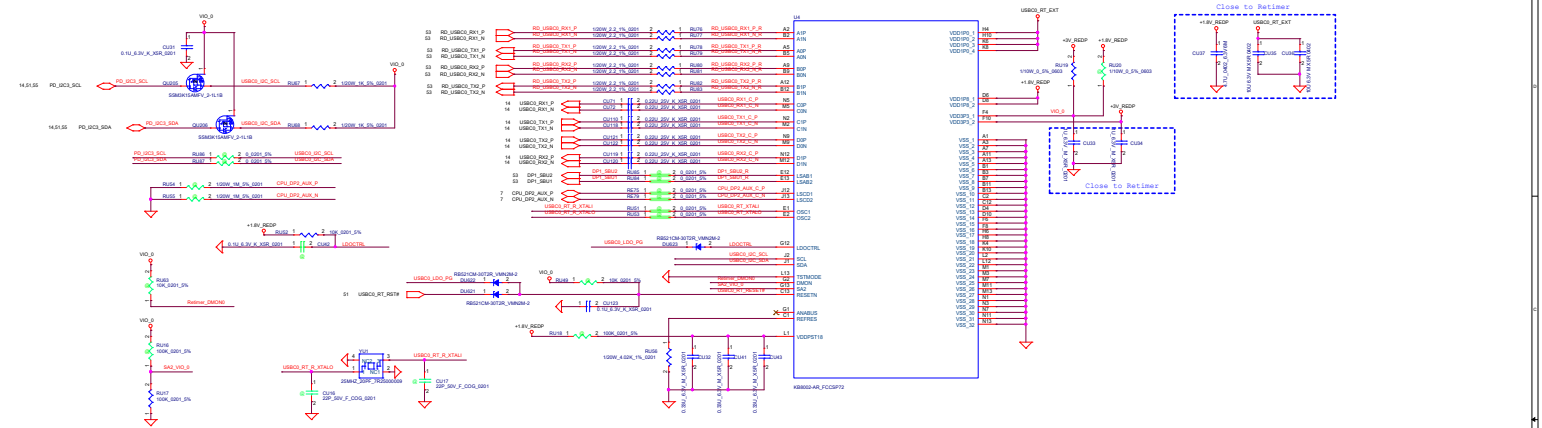


I2C1	Master: EC	PORT A	0x23
	Slave: PD	PORT B	0x27
I2C2	Master: PMC	PORT A	0x23
	Slave: PD	PORT B	0x27
I2C3	Master: PD	PORT A	T.B.D.
	Slave: RT	PORT B	T.B.D.

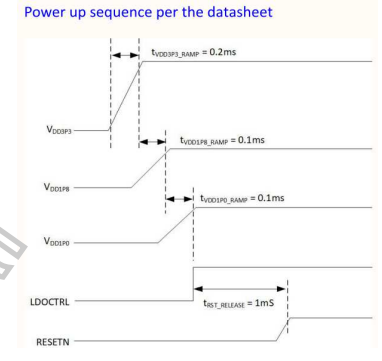
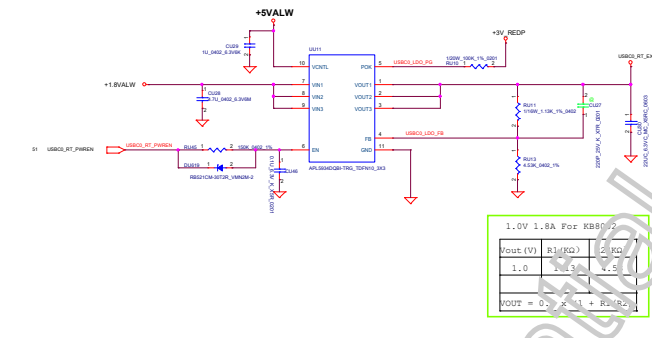
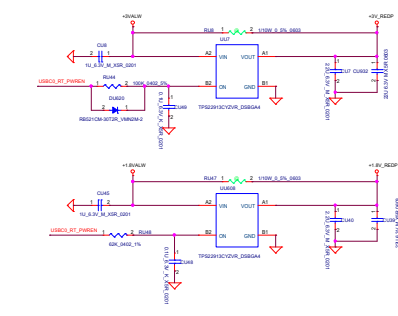
```
ADCIN1 Decoded:2 --0.1079
ADCIN2 Decoded:7 --tie to LDO_3V
I2C Address Index: 4#
```



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Issued Date	2012/07/01	Declassified Date	2014/07/01	
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Rev	Document Number	Date	Issue	Per A
	P081-TYPEC_Controller_PortA	2009-11-06	1	110



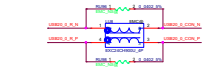
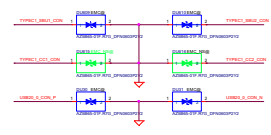
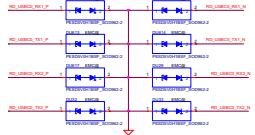
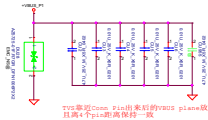
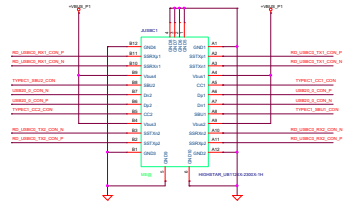
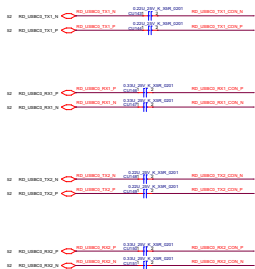
For KB8002:12C slave Address
SA2=0 : 0001 000 (0x08)
SA2=1 : 0001 100 (0x0C)



1.0V 1.8A For KB8002

Vout (V)	I _L (A)	R _{DS(on)} (mΩ)
1.0	1.8	4.5

$V_{OUT} = 0.9 \times V_{IN} + R_{DS(on)} \times I_L$

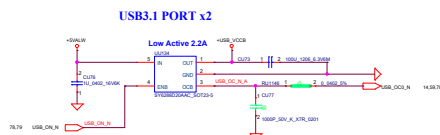


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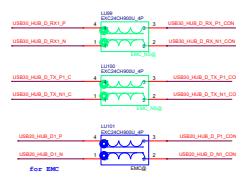
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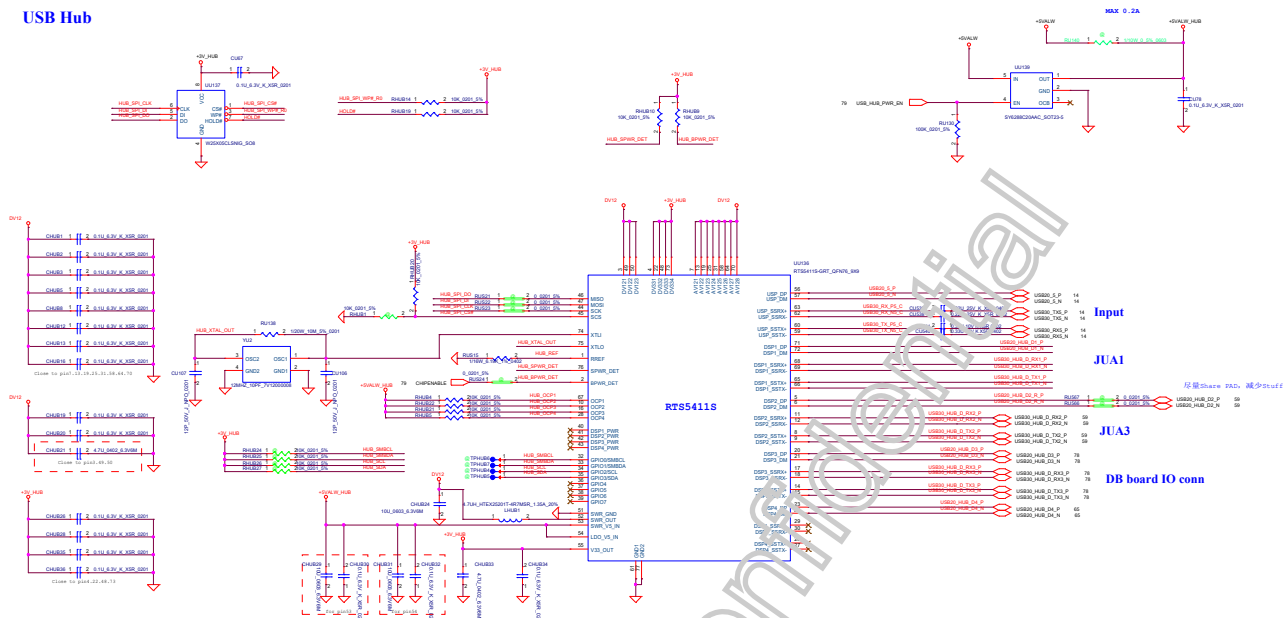
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Del USB Debug Function 0624



USB Hub

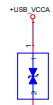
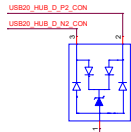
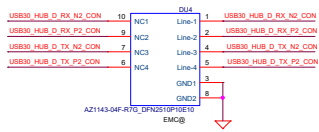
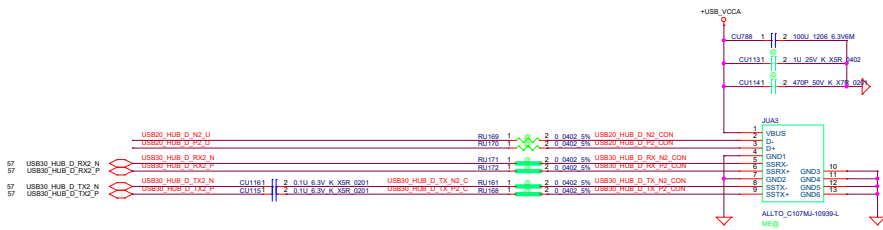


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Serial	E540		18

Delete JUA2 as LNV demmand-0519

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				C	y540
Date				Monday, February 23, 2023	Sheet 35 of 118

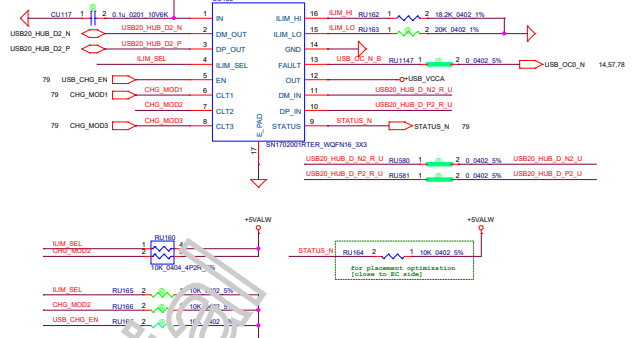
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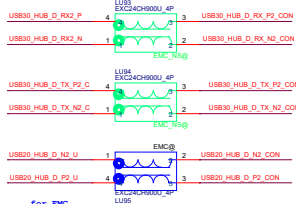
USB charger

2.5A

Follow intel 18.2K-0614



for EMC

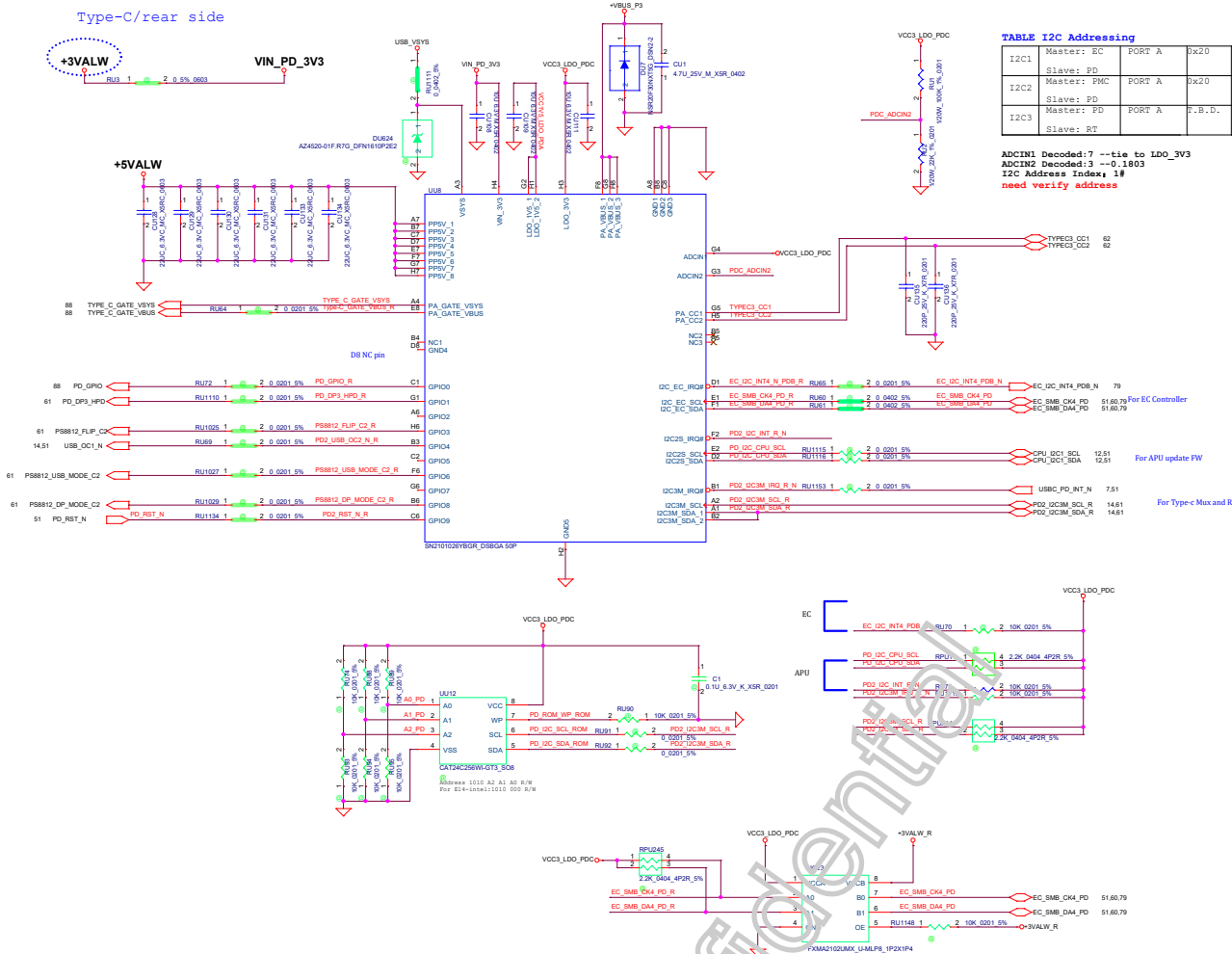


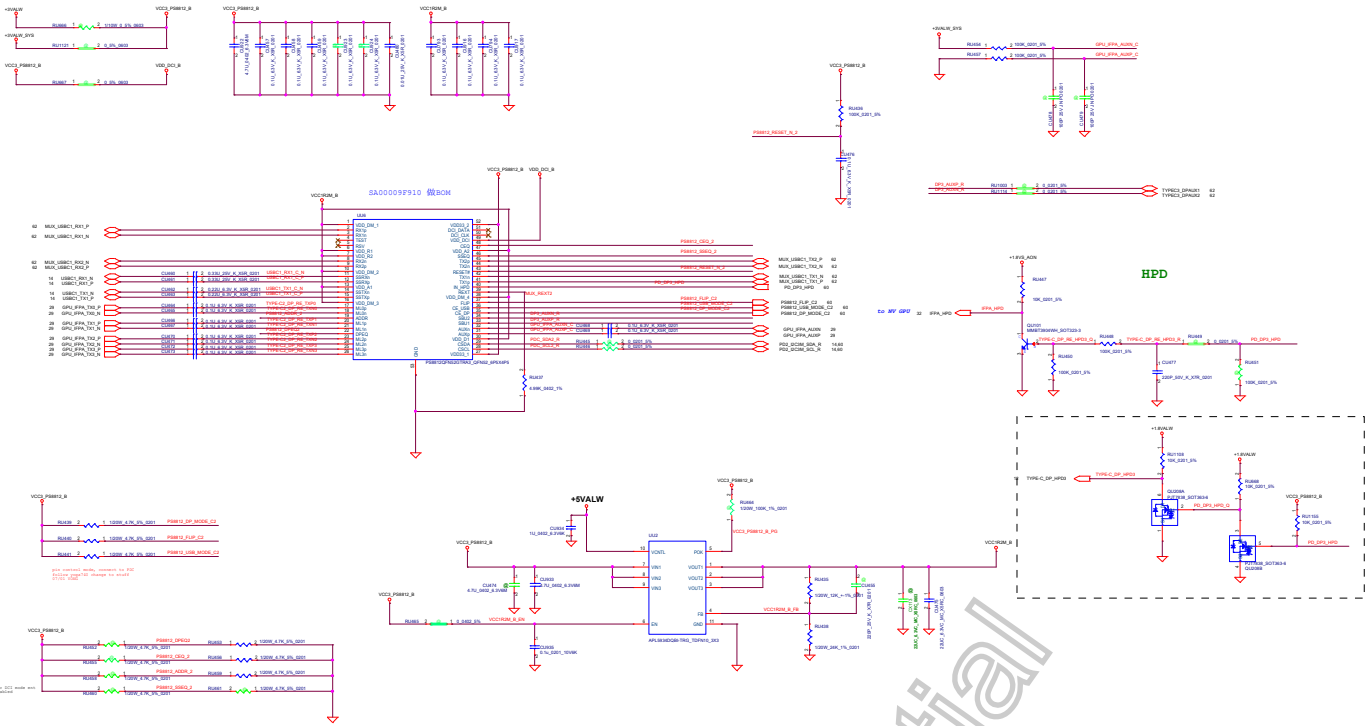
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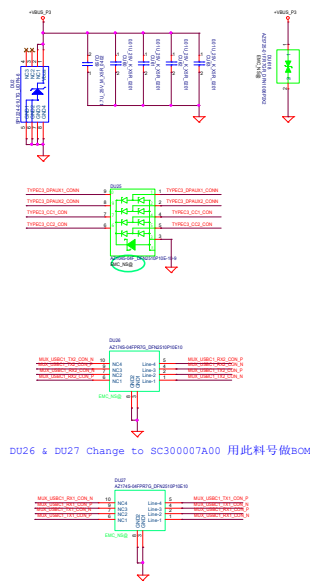
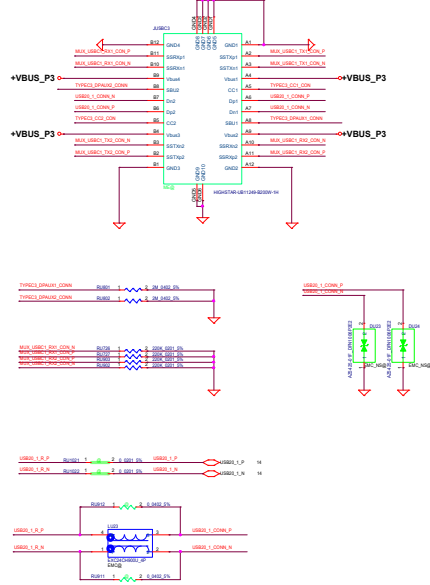
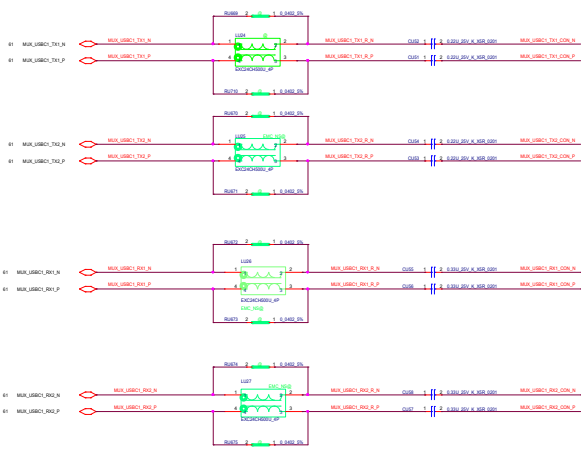
10/14 david modify

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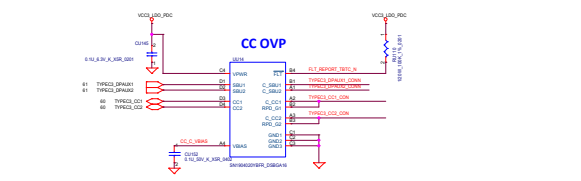
Type-C/rear side



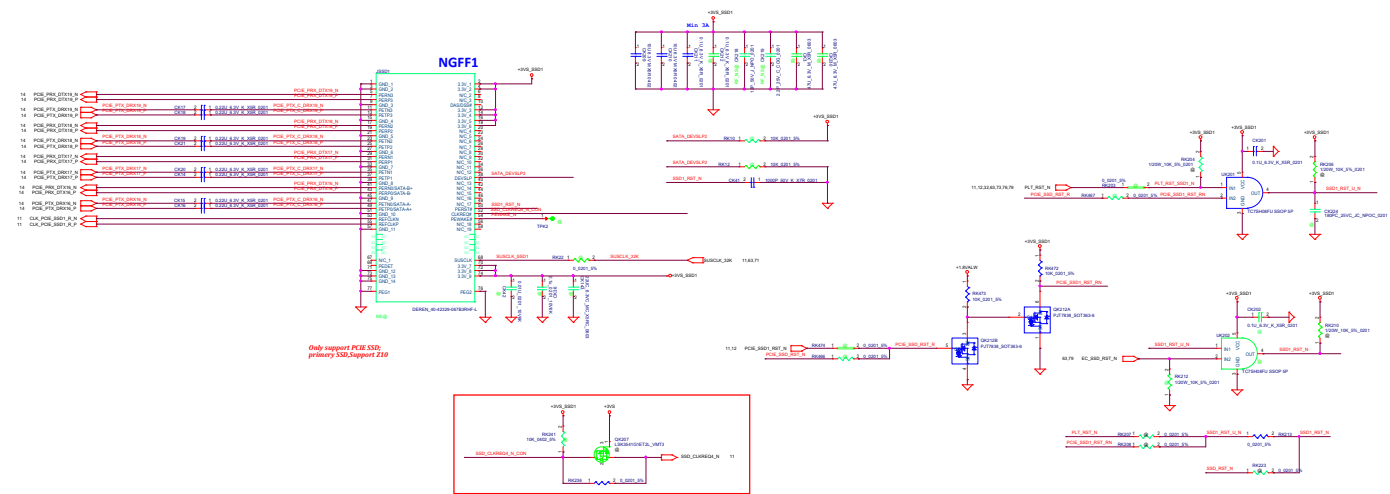




DU26 & DU27 Change to SC300007A00 用此料号做BOM

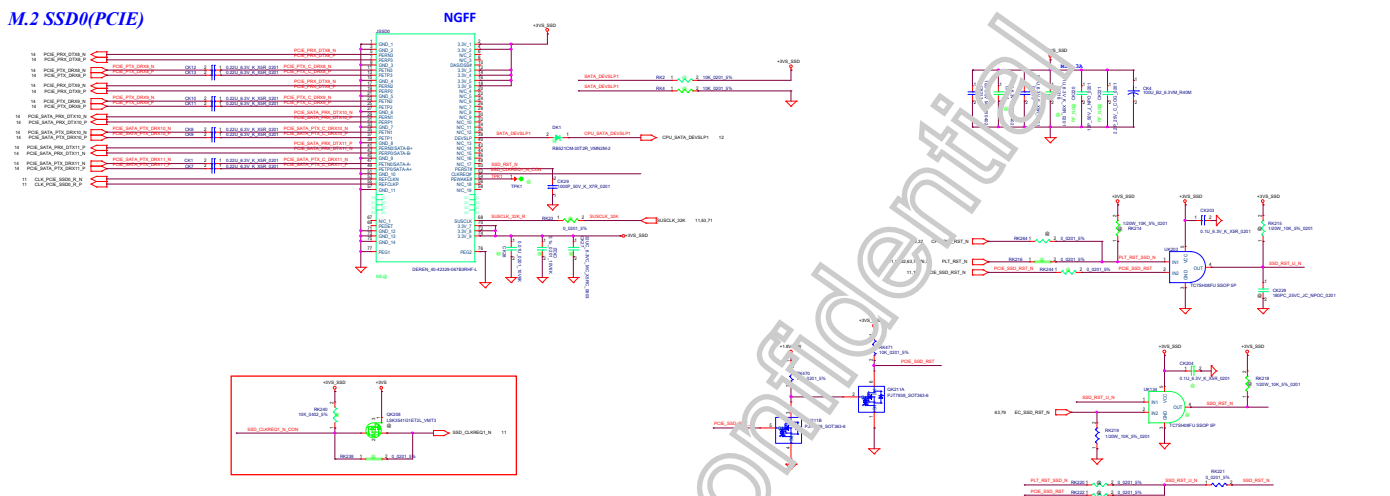


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Only support PCIe SSD
primary SSD Support #19

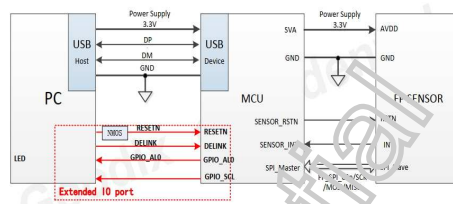
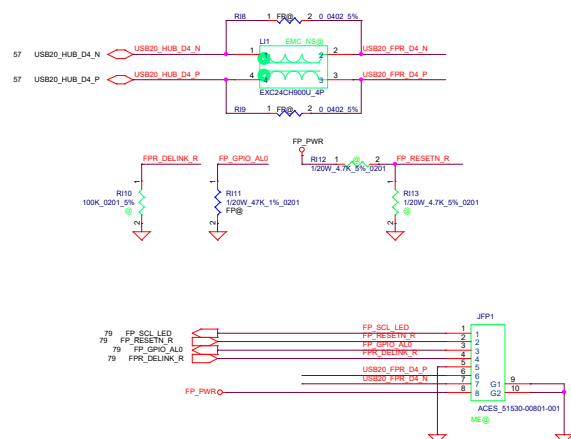
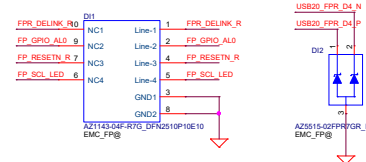
M.2 SSD0(PCIE)



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Secret Date	20180302	Declassified Date	20200302	NGFF WLAN	LCFC
				7540	74

Delete USB3.0 Reapter Remove to DB board

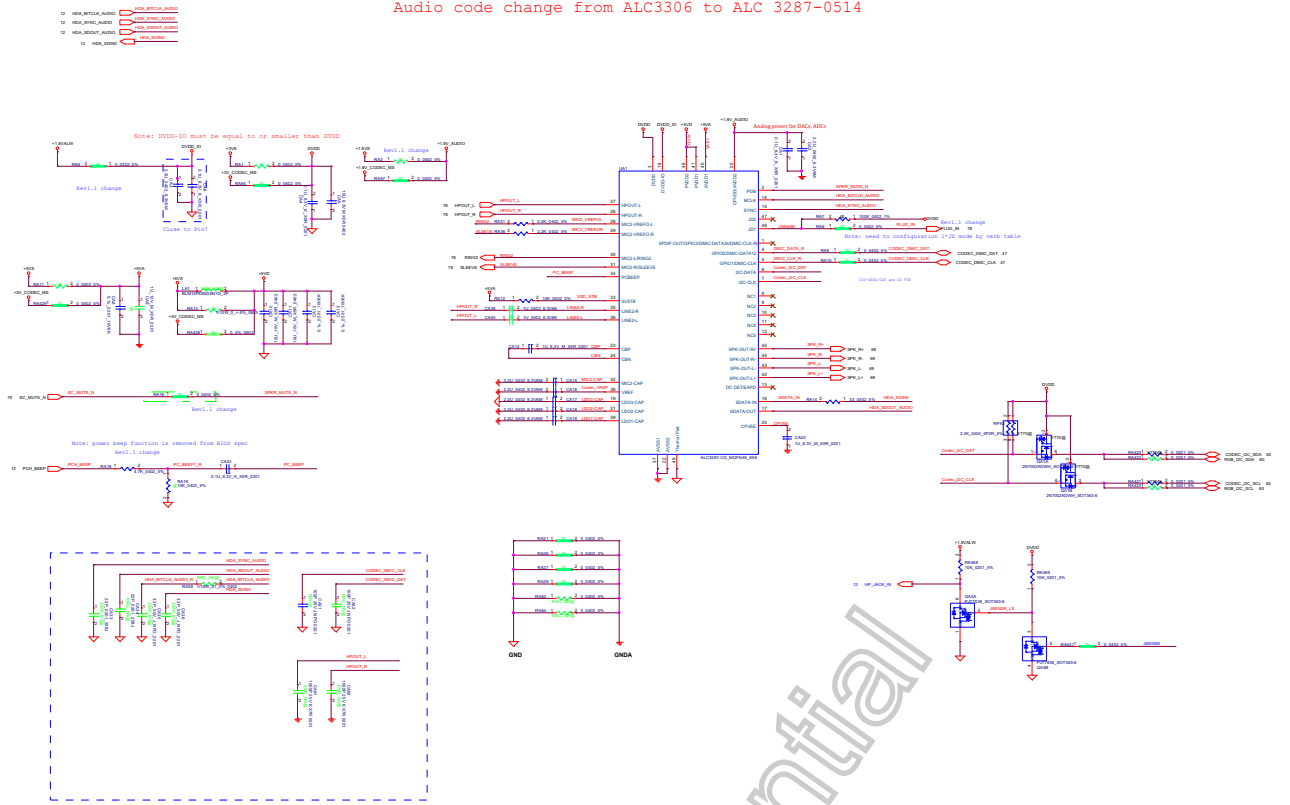
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				Document Number	Y540
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扩展IO接口：	说明：
<ul style="list-style-type: none"> • RESETN：PC输出高电平复位MCU • DELINK：PC输出高电平 • GPIO_ALO：PC输入口，用于电源键屏蔽和控制 • GPIO_SCL：I2C/GPIO复用脚，上电默认I2C_SCL功能，高电平；配置为GPIO后，默认为输入上拉 	<ul style="list-style-type: none"> • 该设备始终支持供电状态 • MCU DELINK、GPIO_ALO、GPIO_SCL默认内部20K上拉

O.	PIN NAME	PIN DEFINE
1	LED	LED控制信号
2	RESETN	MCU 复位信号
3	GPIO_ALO	电源屏蔽
4	DELINK	电源状态指示
5	GND	信号地
5	DP	USB信号DP
7	DM	USB信号DM
3	D3V3	3.3V电源

Audio code change from ALC3306 to ALC 3287-0514



Delete AMP -0514

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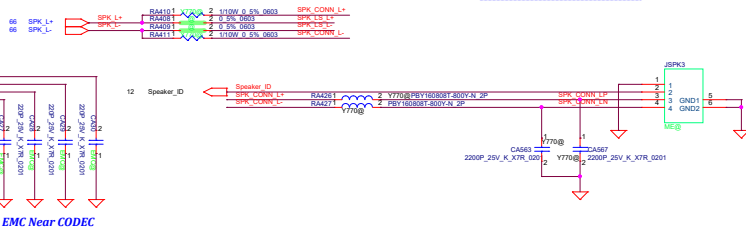
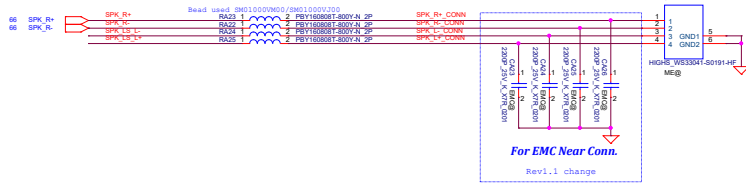
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Issued Date	20091105	Disciplined Date	20091105					
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				Date	Monday, February 27, 2024
				Sheet	95 of 110

Speaker

Speaker



Delete Audio jack and 相关电容电阻,移动到DB小板端-0601

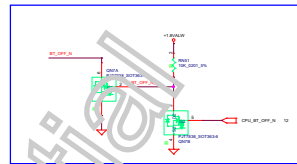
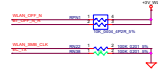
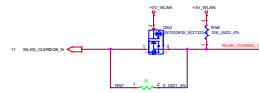
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				Date: Monday, February 23, 2023 Sheet: 35 of 118	

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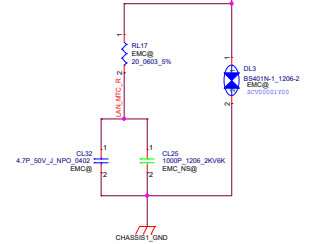
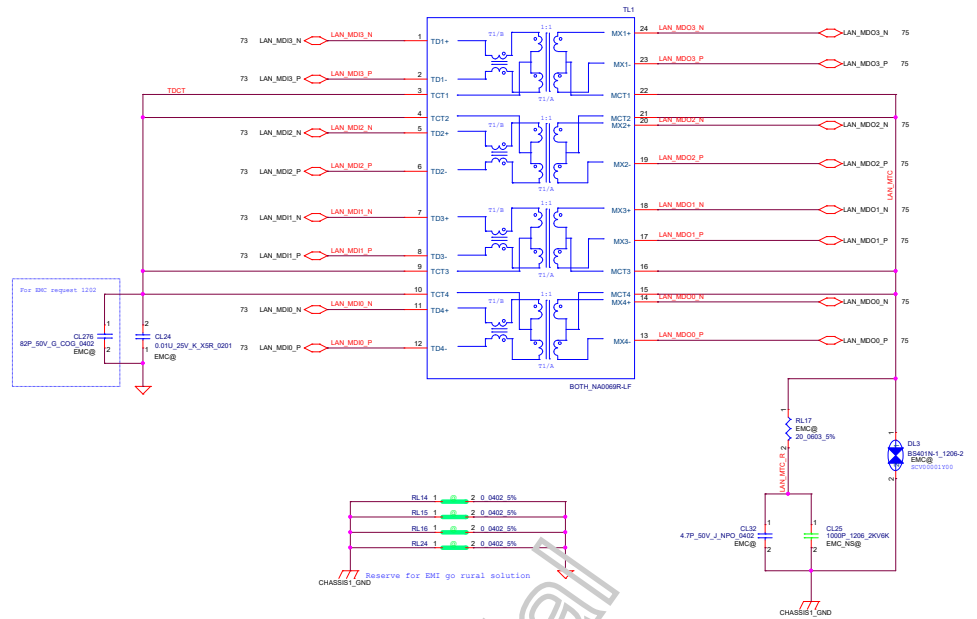
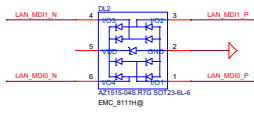
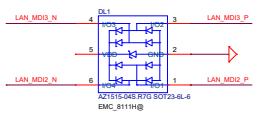
Mini-Express Card(WLAN/WiMAX)
Copy Wlan common design

[illegible]

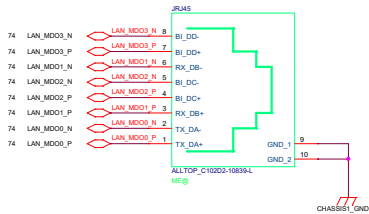
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				Date	2025/02/21/2024
				Sheet	72 of 119

DL1/DL2
1'S PN:SC300005900
Place Close to TL1



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				Date	Monday, February 21, 2023
				Sheet	15 of 115

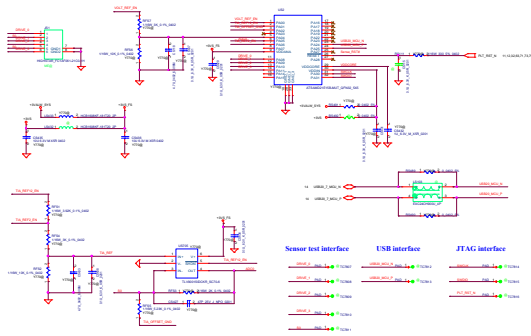


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				Sheet	75 of 110

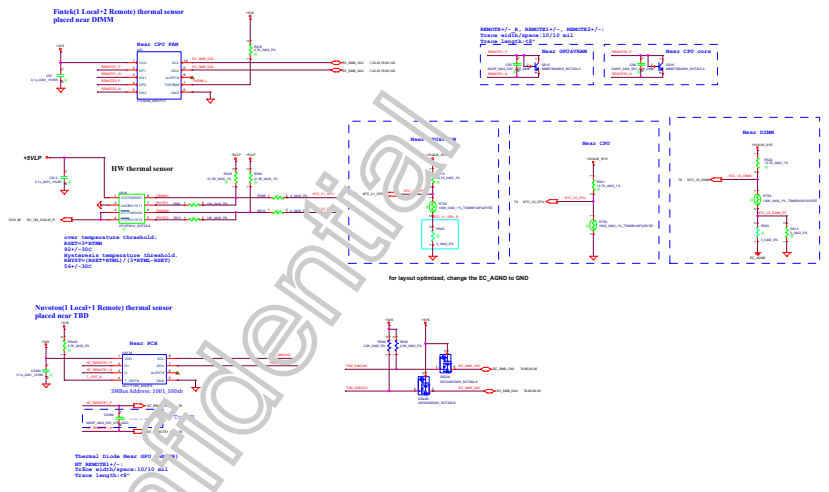
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Delete Senhub for TOF/ALS function canceled--0614

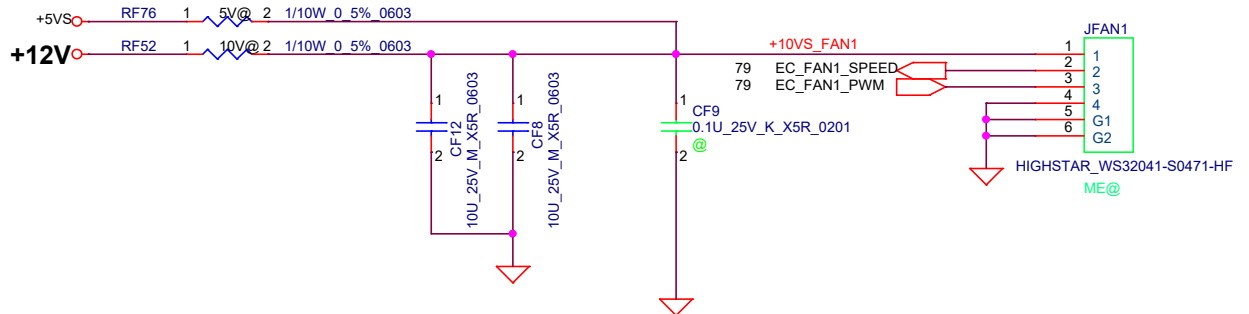
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Thermal Sensor

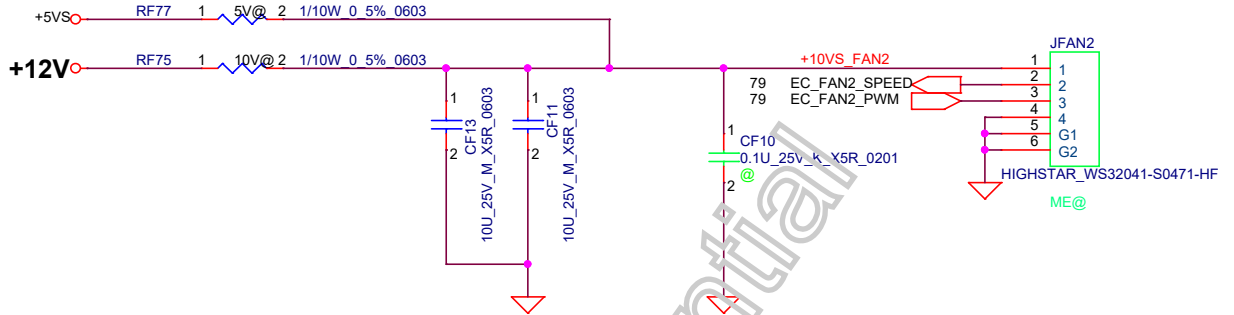


FAN Conn Right



22U 电容换成两颗100 0603 电容 TOP 和BOT各放一颗
怎加5V 供电，各加两颗100电阻

FAN Conn LEFT

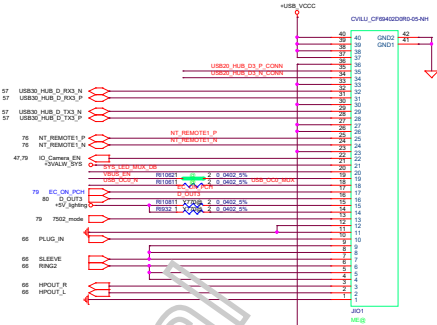
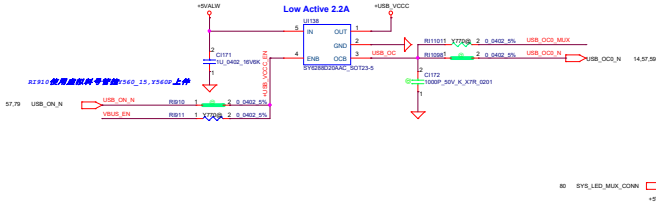


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A		Y540									

Right Side USB2.0 Port X 1 (USB/B)

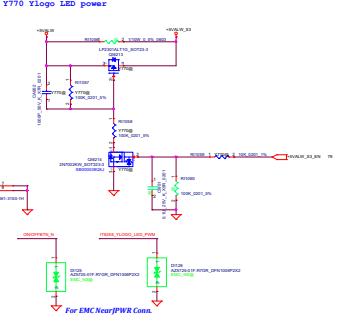
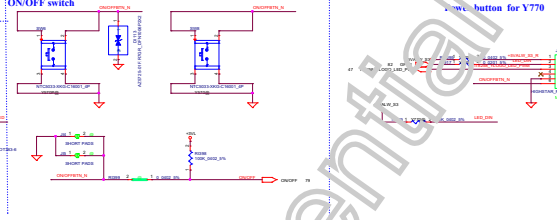
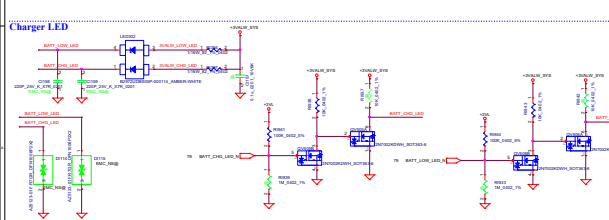
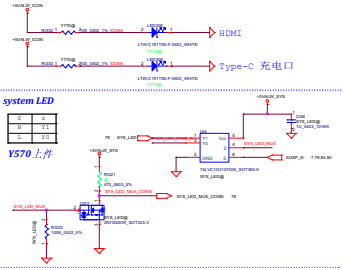
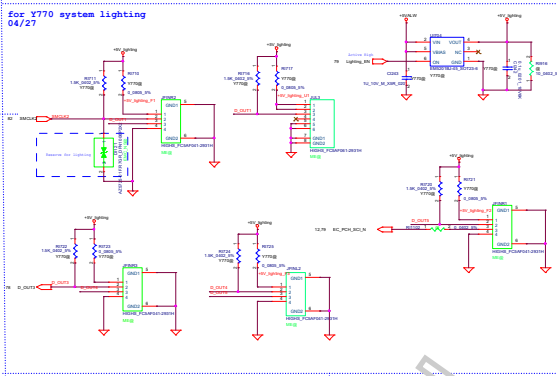
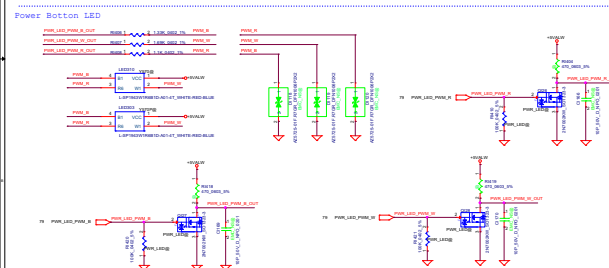
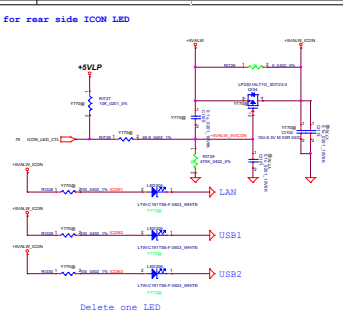
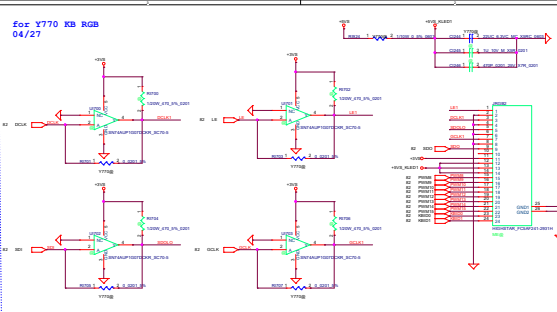
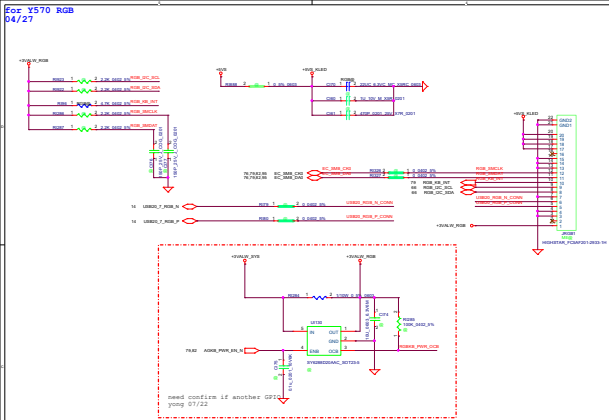


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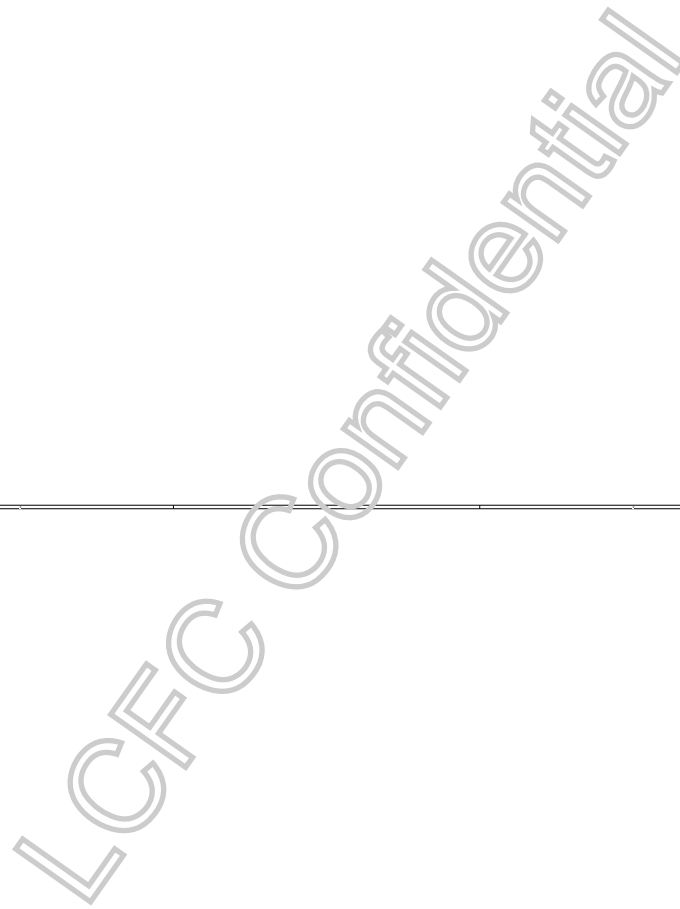


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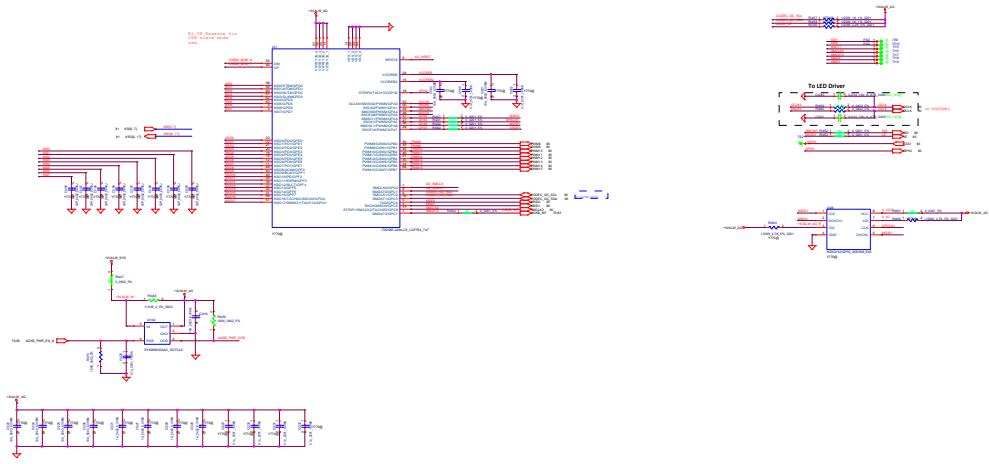


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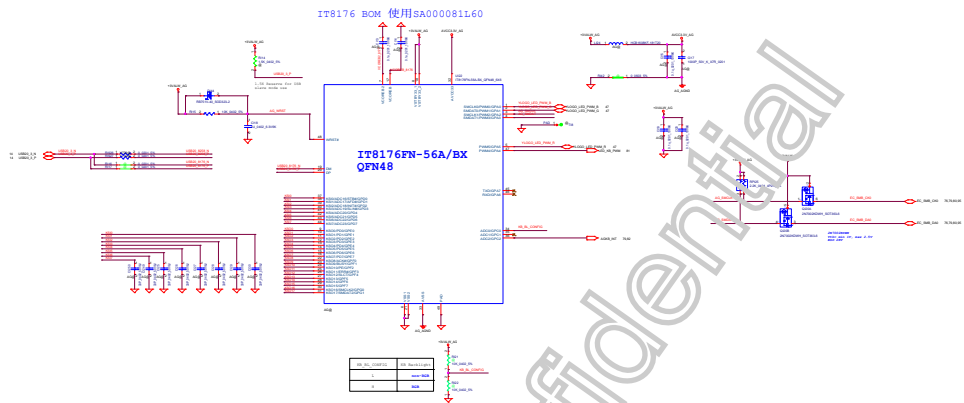


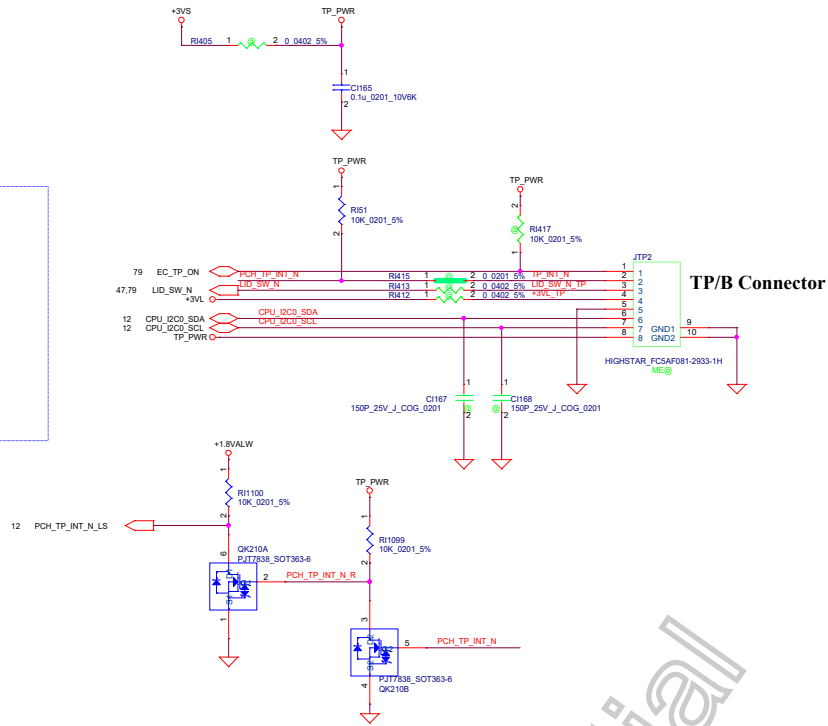
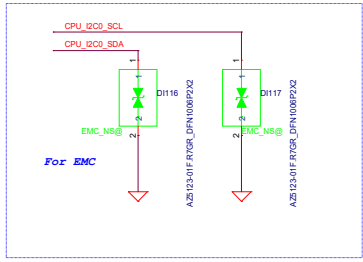
LCFC

IT8258

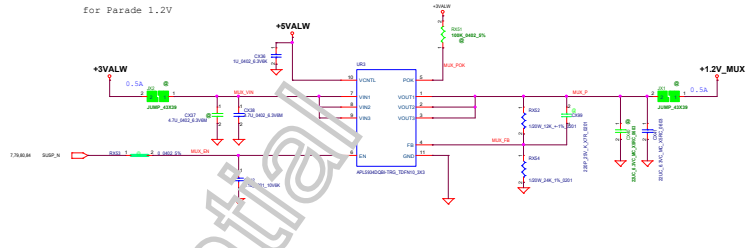
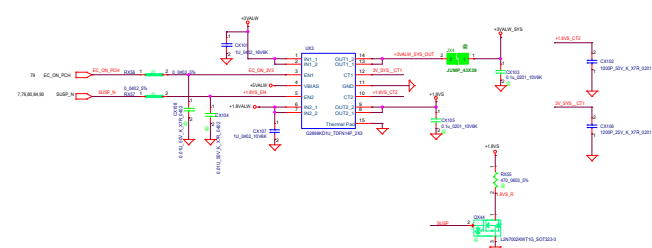
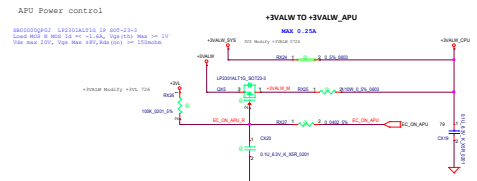
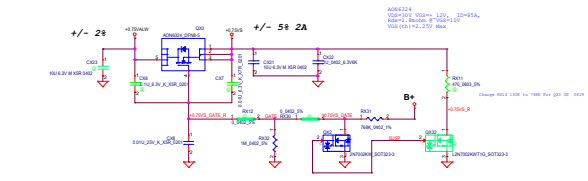
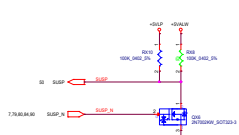
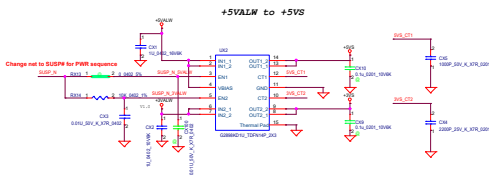


IT8176



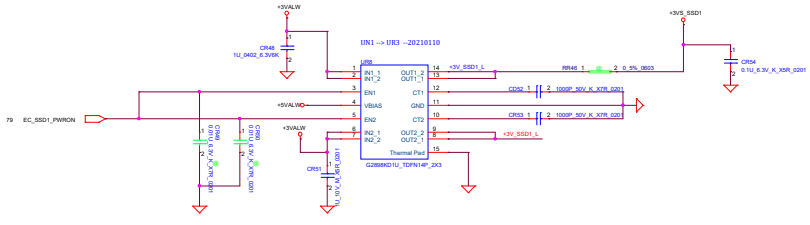


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Monday, February 21, 2022		83		110	

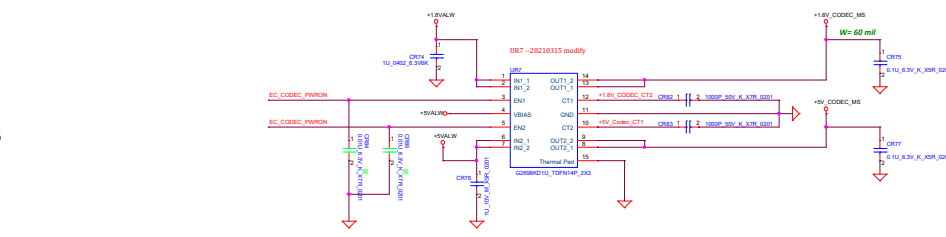
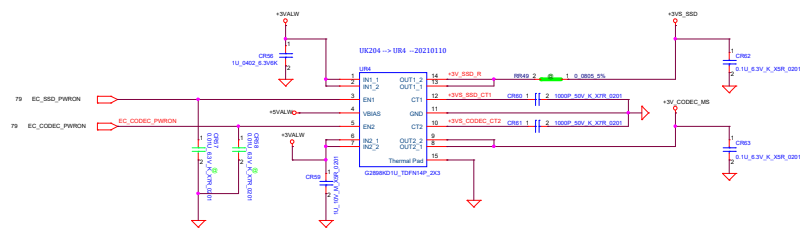


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Doc Rev	1.0	Doc Date	20180918

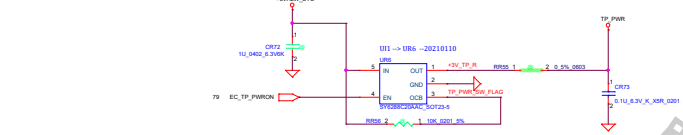
SSD1 PWR Control



SSD & Codec MS PWR Control

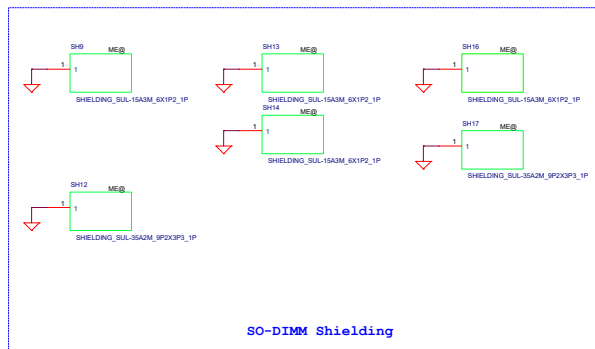
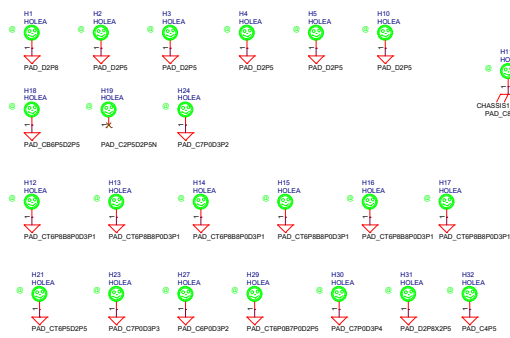


TP MS Power control

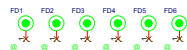


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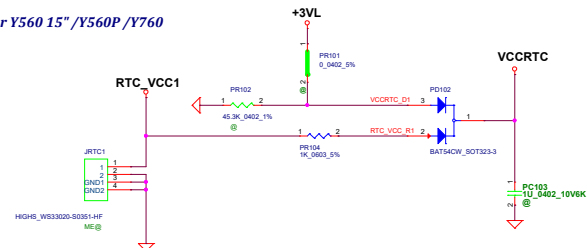



SO-DIMM Shielding



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ACDET Threshold:min:17.878V
BAT Max V=17.6V

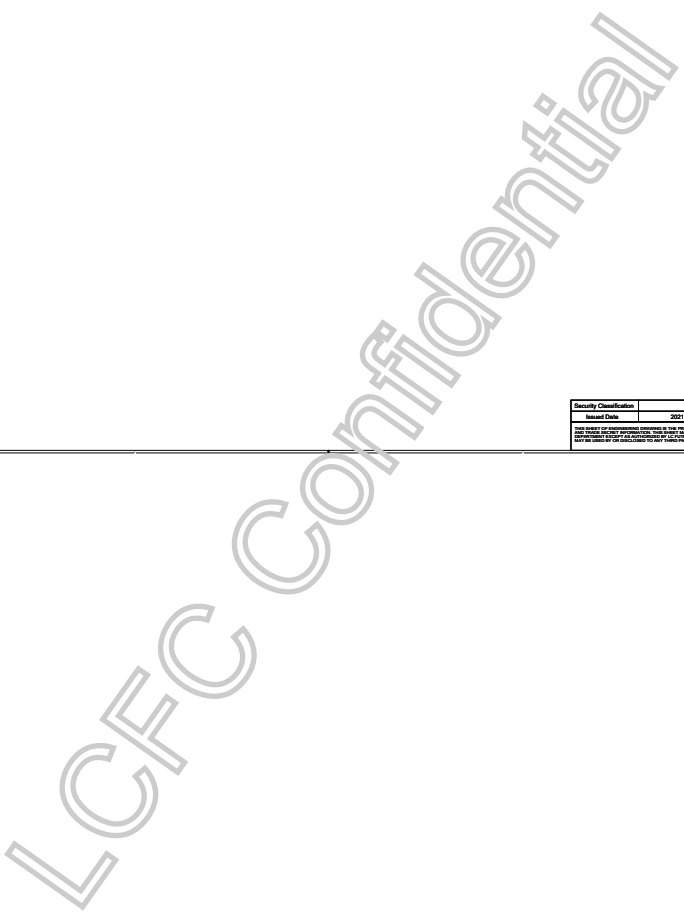
PMON Gain=1uA/W Actuacl=0.5uA/W
PR5415=15K 0.75V=100W

IchargeLim=17.6A
IchargeLim=70.4A

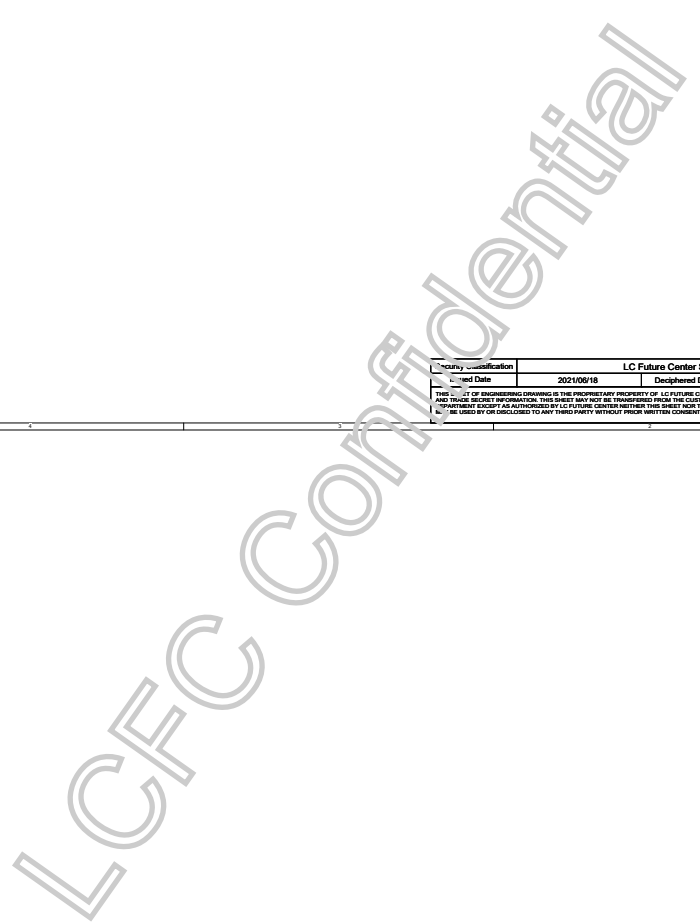
For Charge current -16A


V charge (MAX):17.6V
I charge (MAX):16A
FSW:800K

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01	2021/06/18	01	2021/06/18	Y570	
PWR-charger					01
Monday, February 21, 2023					01



```
Vout=5V+-5%
Vset=5.06V+-1.5%
FSW=500KHz/5V; 600K/3.3V
TDC=20A OCP=26A
OVP=Vout*113%
UVP=Vout*52%
```



Title		Y570 AMD			
Site Custom	Document Number	SVALW_DDR5			Rev 6.1
Order	Monday, February 21, 2022	Release	95	of	115

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				Document Number	
C				PWR_Memory PWR Decoupling	
Date				Monday, February 21, 2023	Sheet 95 of 110

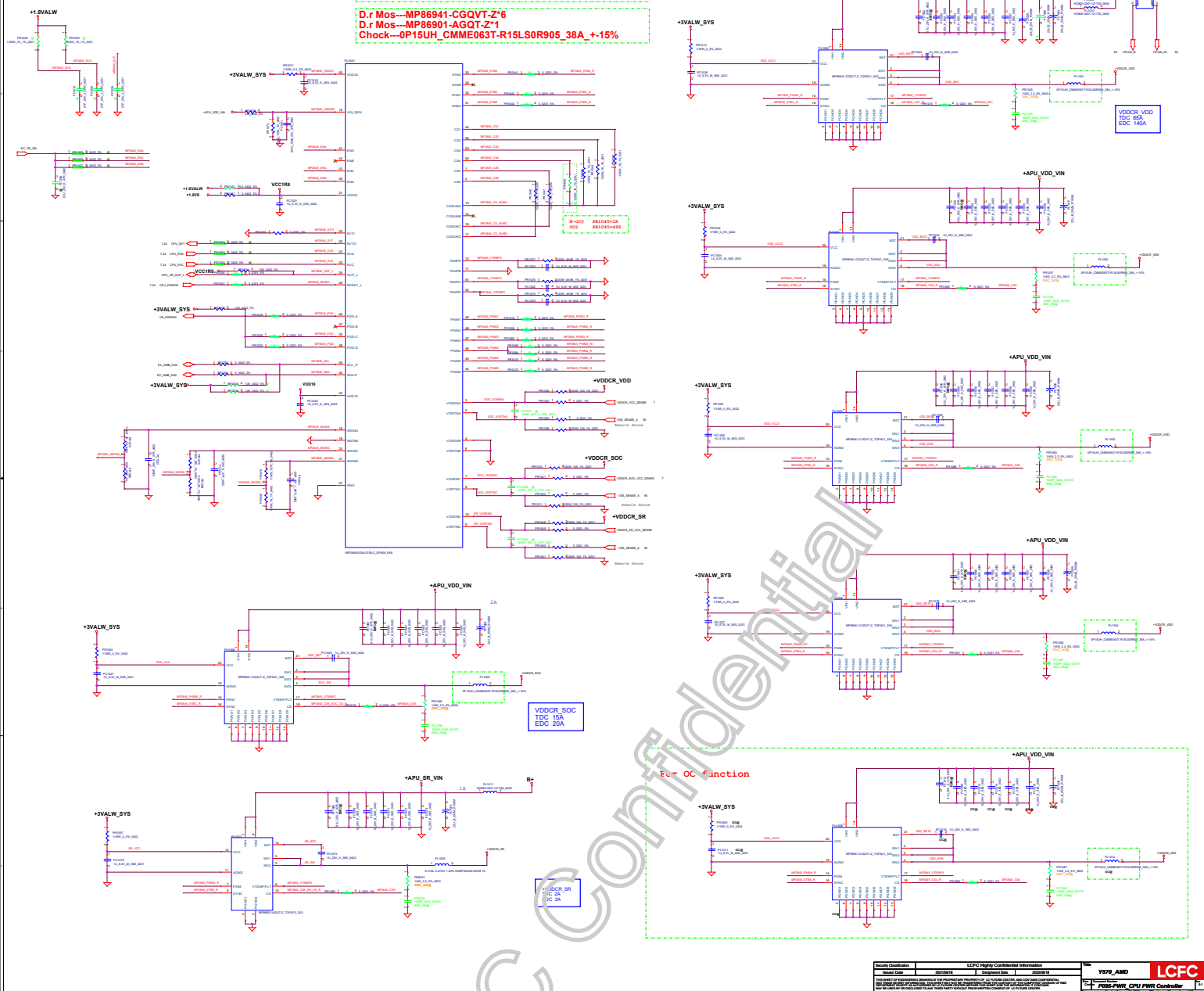
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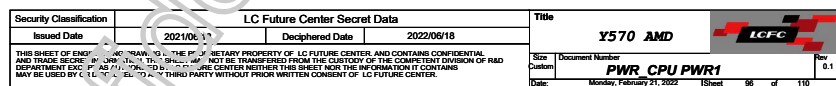
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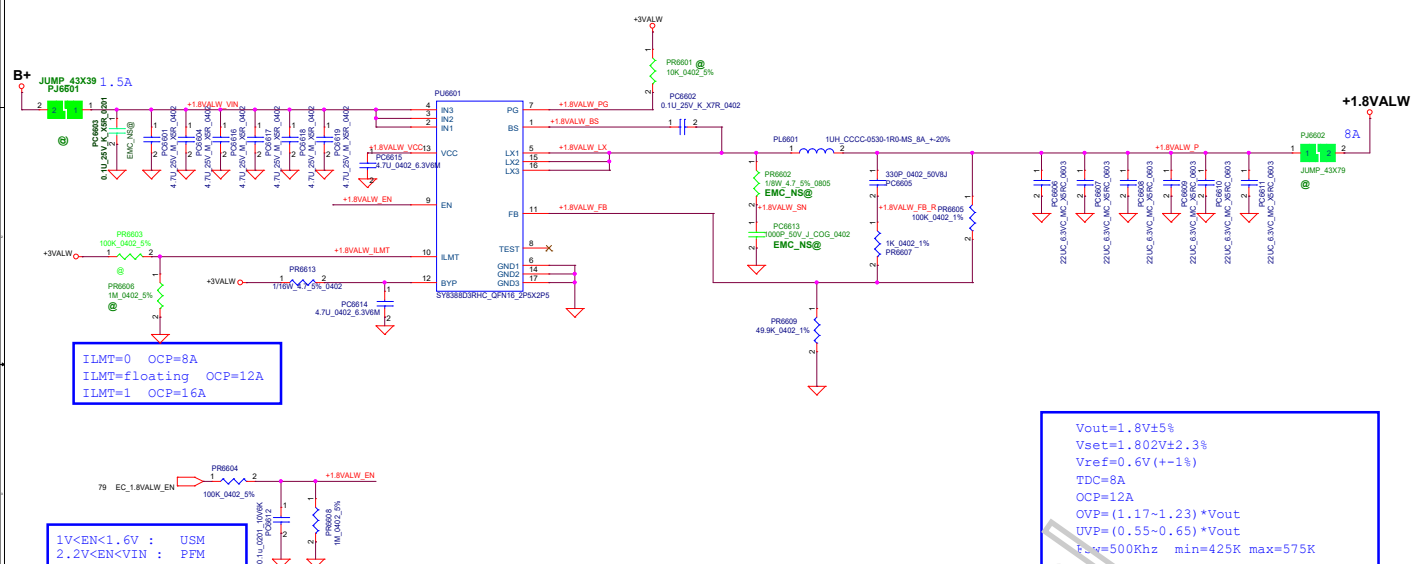
D.r Mos---MP86941-CGQVT-Z*6

D.r Mos---MP86901-AGQT-Z*1

Chock---0P15UH_CMME063T-R15LS0R905_38A_+15%







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ALL BU(on top side under CPU



All BU (on top side under CPU)



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Date		Monday, February 23, 2023		Sheet	95 of 115



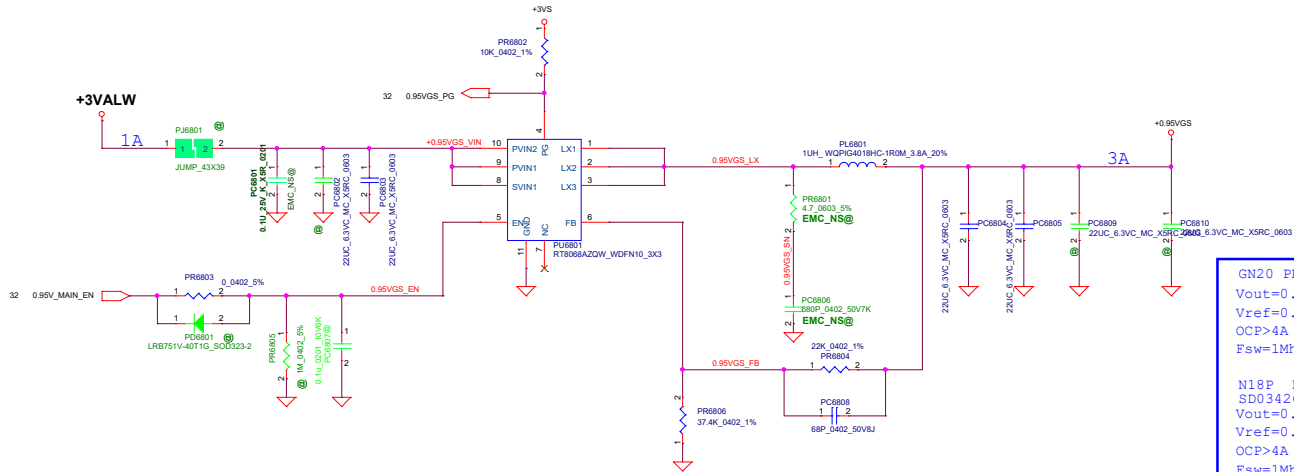
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				PCH PWR2	
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				C	PWR_PCH PWR Decoupling
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GN20 PR6804=22K
 Vout=0.953V±3%
 Vref=0.6V
 OCP>4A
 Fsw=1Mhz

 N18P PR6804=26.1K
 SD03426128J
 Vout=0.953V±3%
 Vref=0.6V
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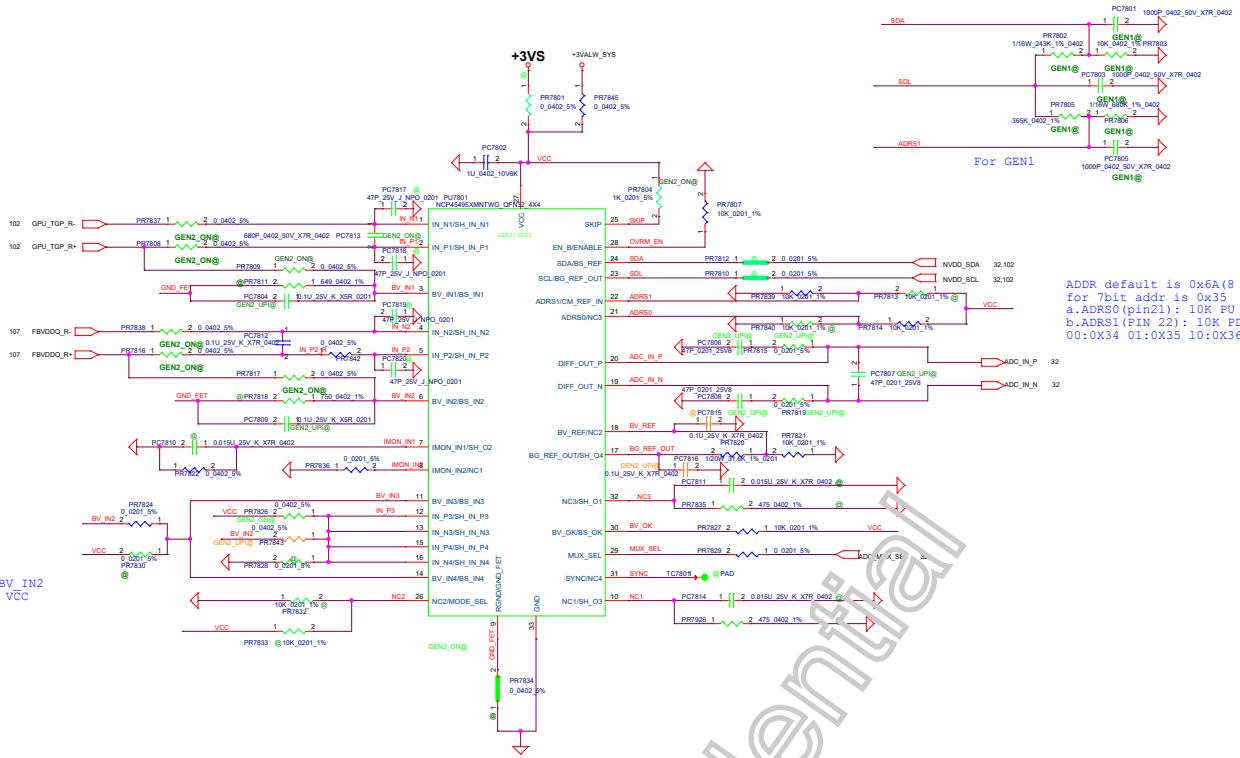
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				Custom	PWR_GPU PWR
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				Custom	PWR_GPU PWR2	0.1		
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BV_INX ON BV_IN2
UPI VCC



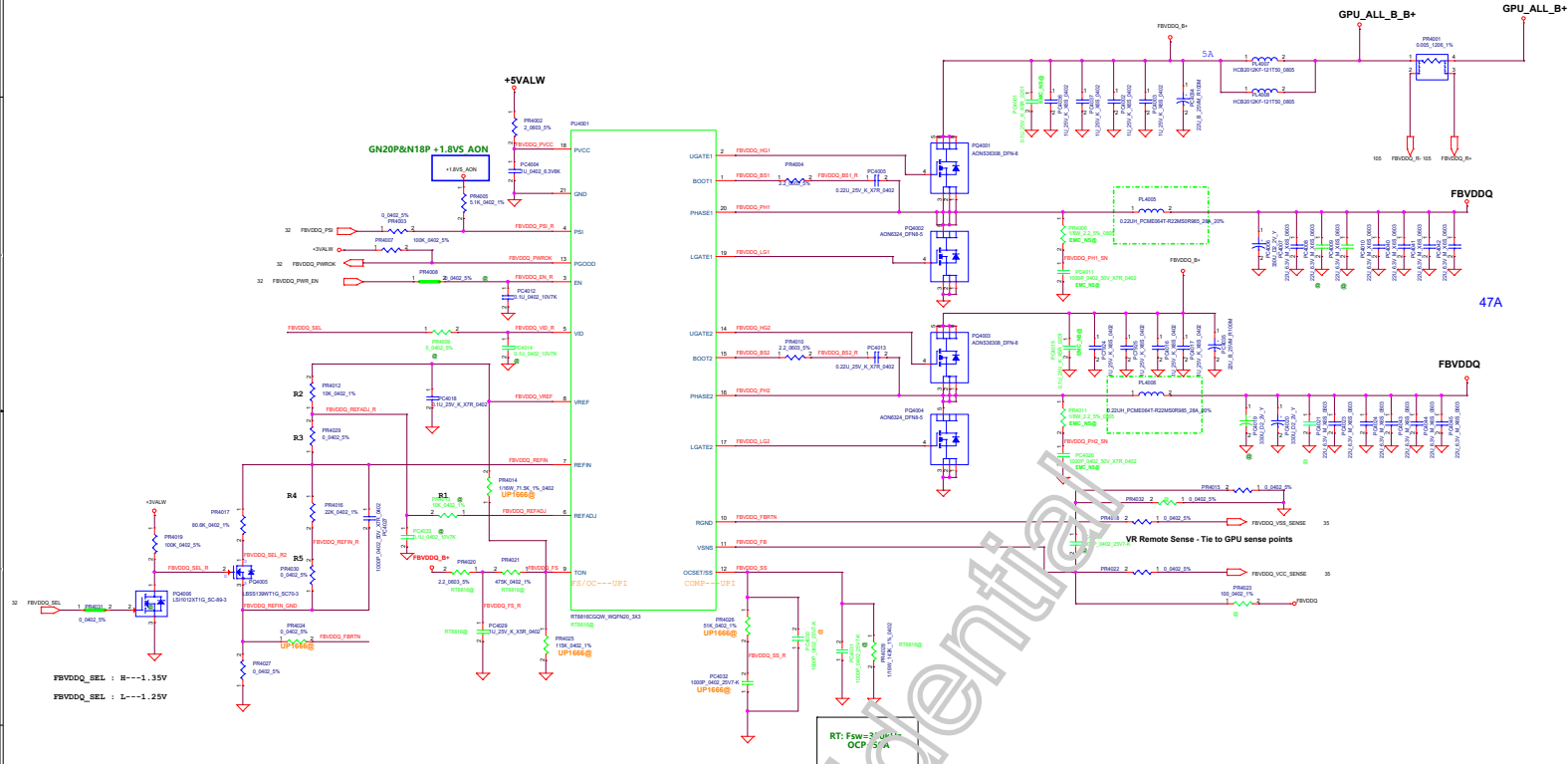
ADDR default is 0x6A(8 bit addr),
for 7bit addr is 0x35
a.ADDRS0(pin21): 10K PU 3.3v
b.ADDRS1(PIN 22): 10K PD to GND
00:0X34 01:0X35 10:0X36 11:0X37

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				Date	Monday, February 22, 2021

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RT8816 PSI	UP1666 PSI	Phase Configuration
1.0V~5.3V	1.4V~5.3V	2Phase CCM
1.0V~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM



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				C	Change List_PWR
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